Low-Jitter PLLs for Wireless Transceivers

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Outline

- **PLL Basics**
- Classical CP PLL Analysis and Optimization
- Low Jitter Sub-Sampling PLL Architecture
- Frac-N Sub-Sampling PLL
- Conclusion

PLL and Applications

- PLL is short for Phase Locked Loop, a feedback control system that generates an output signal whose phase is locked to the phase of an input signal

- PLLs are versatile
  - Clock generation
  - Frequency synthesis
  - Phase/Frequency modulation
  - Clock and data recovery
  - Synchronization

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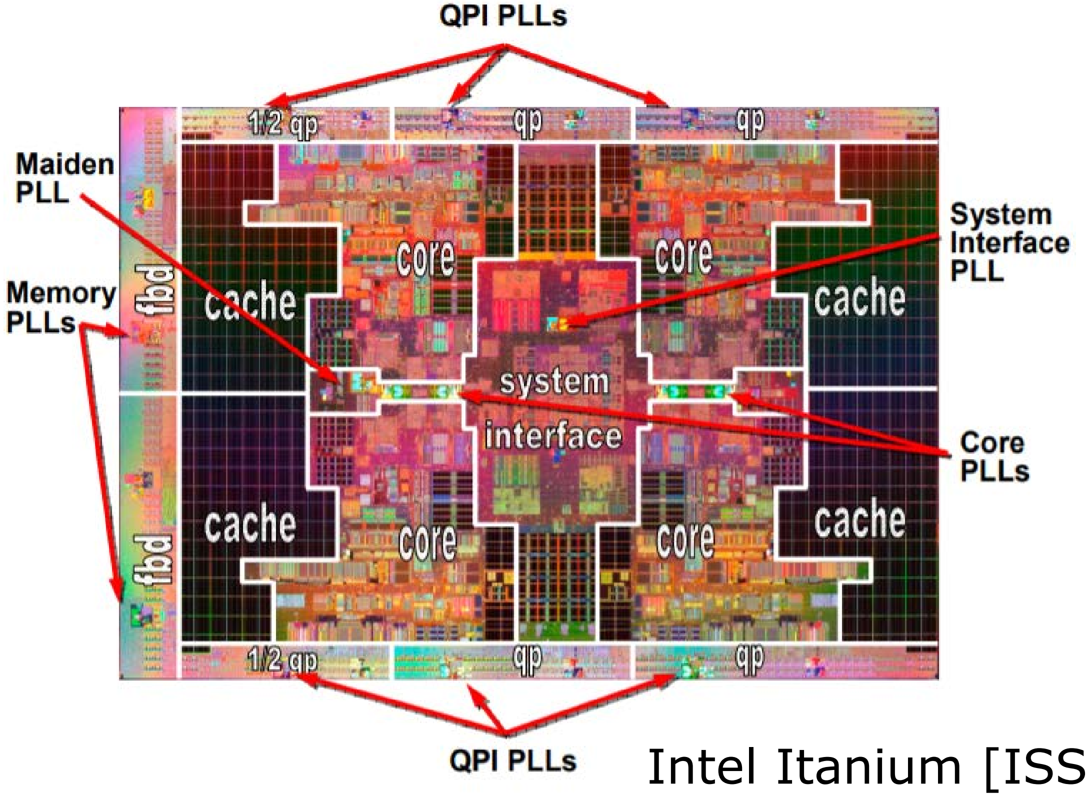
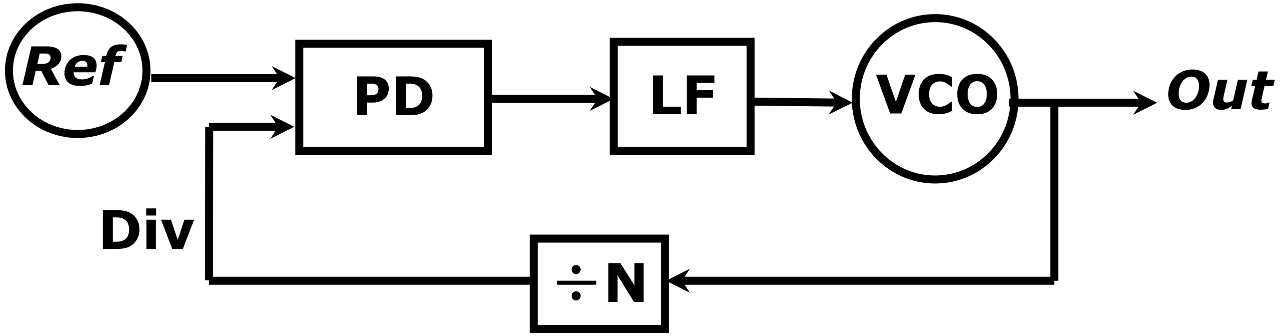
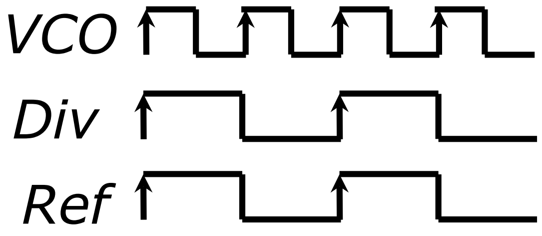


Intel Itanium [ISSCC09]

Basic PLL Architecture



- Basic components in a PLL
  - Reference clock (Ref)
  - Phase Detector (PD)
  - Loop Filter (LF)
  - Voltage Controlled Oscillator (VCO)
  - Frequency Divider (÷N)



Phase Locked

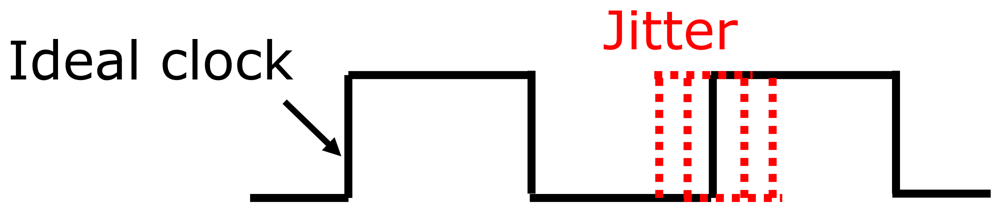
PLL Performances Metrics

- PLL performance can be measured in many ways:
  - Phase Noise
  - Jitter
  - Power Consumption
  - Spur
  - Settling Time
  - Locking Range
  - Silicon Area

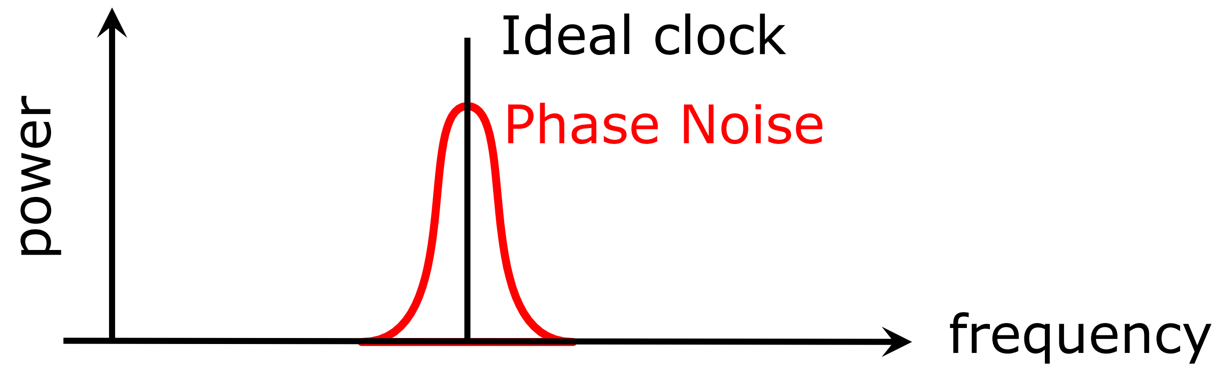
  …
- This tutorial emphasizes on phase noise / jitter and power as they involve fundamental tradeoffs and are often key PLL design specs for wireless transceivers

Jitter and Phase Noise

- Jitter is the random or systematic deviation in time of the zero-crossings of a clock with respect to corresponding zero-crossings of an ideal clock

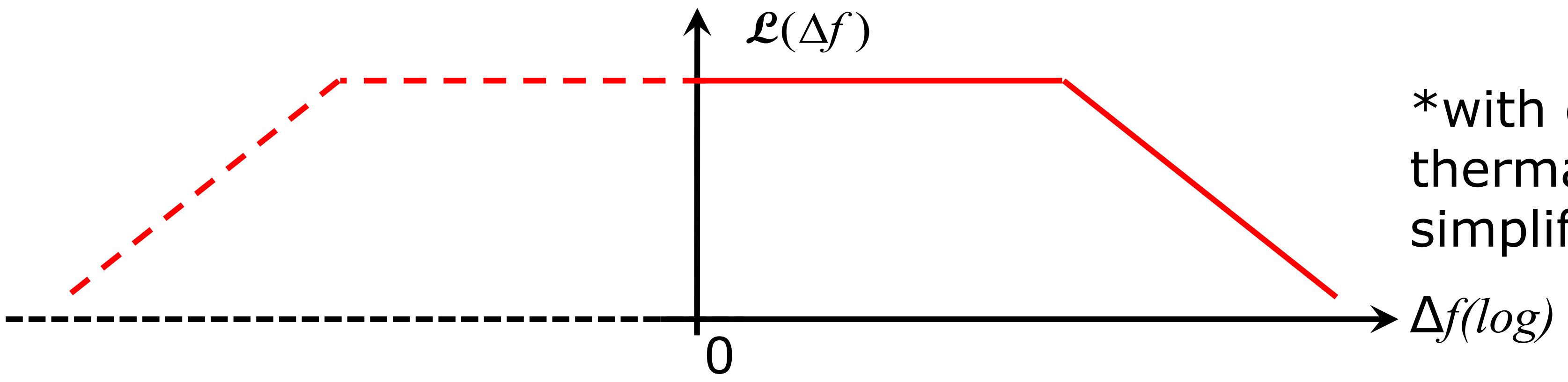


- In frequency domain, the deviation from ideal clock result in spectral components at frequencies other than the intended output frequency, i.e., phase noise



Relating Jitter and Phase Noise

- Phase Noise is often expressed in single-sideband-noise-to-carrier ratio $\mathcal{L}(\Delta f)$, which is half the one sided power spectral density S_{Φ}, at offset frequency Δf relative to the carrier, plotted in dB scale with unit dBc/Hz :

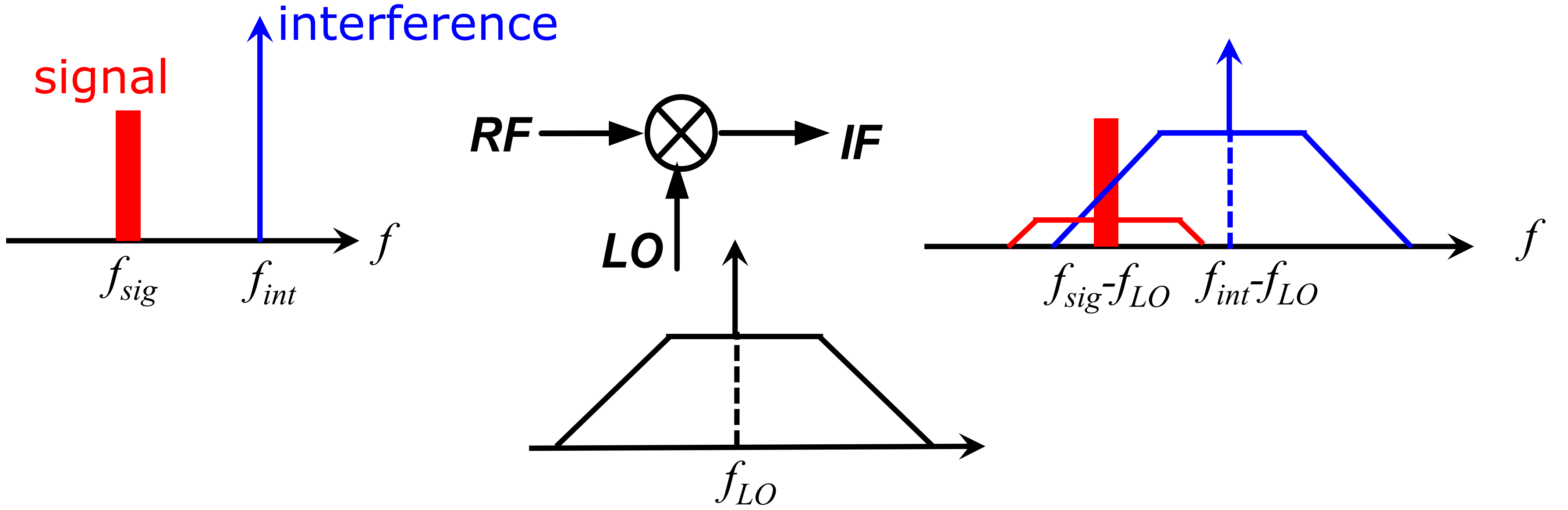


*with only thermal noise to simplify analysis

- Total rms phase error is the integral of $\mathcal{L}(\Delta f)$: $\sigma_{\Phi}^2 = 2 \times \int_0^{\infty} \mathcal{L}(\Delta f) df$
- Rms jitter is related to rms phase error as:

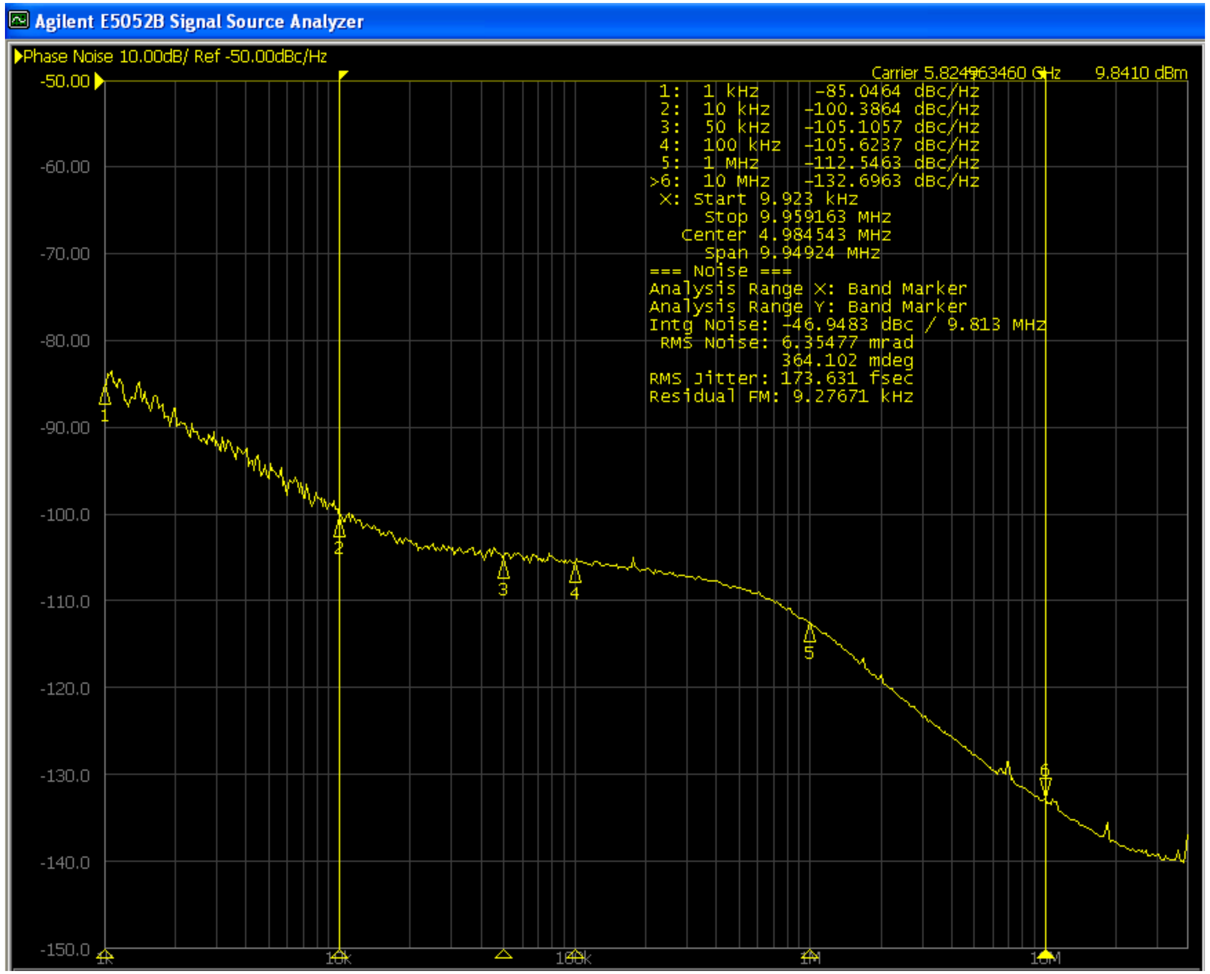
$$\frac{\sigma_t}{T_{out}} = \frac{\sigma_{\Phi}}{2\pi} \Rightarrow \sigma_t = \frac{\sigma_{\Phi}}{2\pi f_{out}} \quad \text{thus} \quad \sigma_t^2 = \frac{2 \times \int_0^{\infty} \mathcal{L}(\Delta f) df}{(2\pi f_{out})^2}$$

Impact of Phase Noise In Wireless Transceivers



- In wireless transceivers, PLL is often used to generate Local Oscillator (LO) clocks for the mixer
- In receiver, reciprocal mixing of LO phase noise and interferences fall into signal band and degrade SNR. This translates to a spec of total phase error or jitter integrated over a band of interest [f_l, f_h]. E.g. [10kHz,10MHz] for 802.11n WLAN

Phase Noise Spectrum Example



f_l=10kHz f_h=10MHz

- From the signal source analyzer, we can read

Carrier Freq	**5.825GHz**
PN at 10kHz	**-100.3dBc/Hz**
PN at 100kHz	**-105.6dBc/Hz**
PN at 1MHz	**-112.5dBc/Hz**
PN at 10MHz	**-132.6dBc/Hz**
Intg Noise (10kHz,10MHz)	**-46.95dBc**
RMS Noise	**6.35 mrad, 364.1mdeg**
RMS Jitter	**173.6 fsec**

Phase Noise / Jitter Calculation Example

- In this example, single side phase noise integrated from 10KHz to 10MHz is -46.95dBc, the rms phase error is:

$$\sigma_{\Phi} \approx 10^{(-46.95+3)/20} \approx 6.35\text{mrad}$$

or $$\frac{6.35m}{2\pi} \times 360 \approx 364\text{mdeg}$$

- The rms jitter can be calculated as:

$$\sigma_t = \frac{\sigma_{\Phi}}{2\pi f_{out}} = \frac{6.35m}{2\pi \times 5.825GHz} \approx 173.6\,fs$$

Carrier Freq	**5.825GHz**
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- Low Jitter Sub-Sampling PLL Architecture
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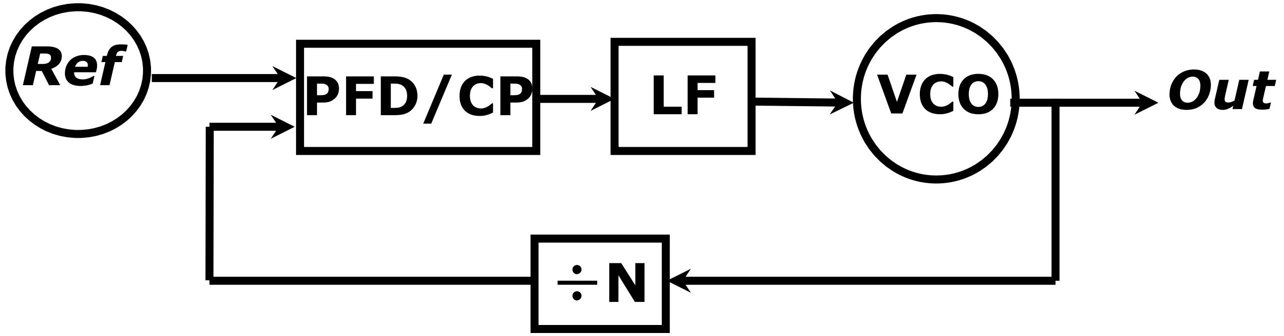
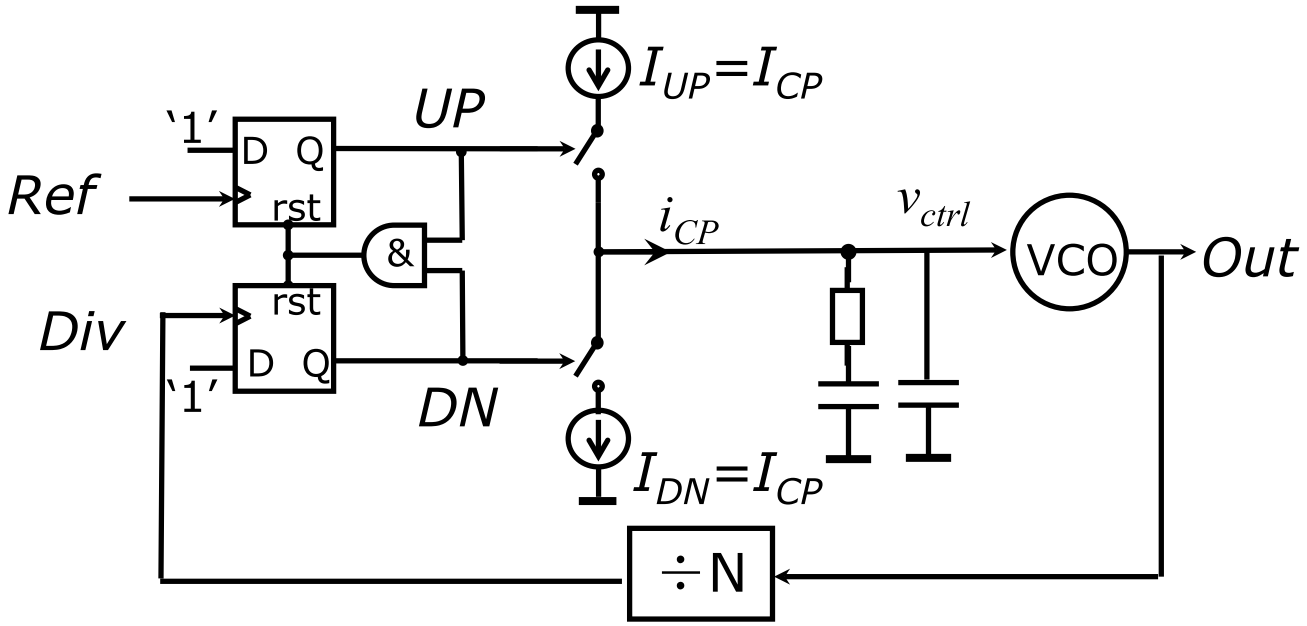
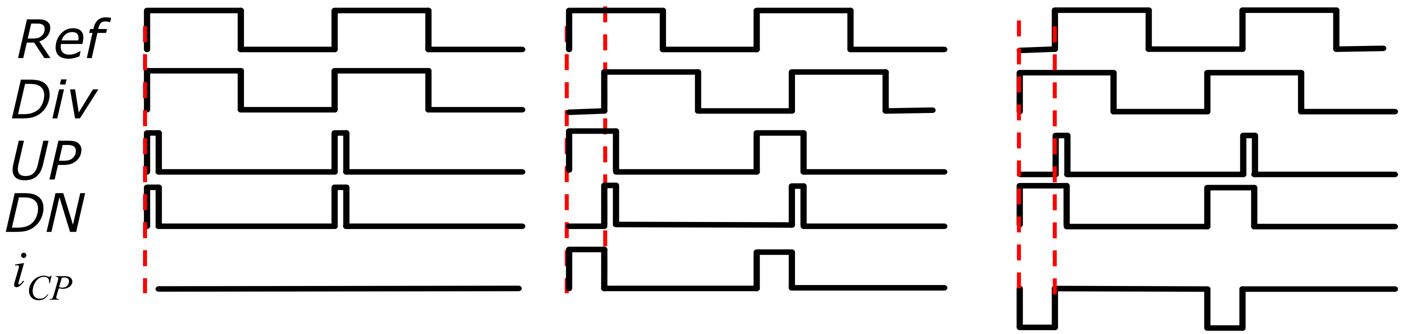
Classical CP PLL Architecture



- Components in a classical CP PLL
  - Reference clock (Ref)
  - Phase Frequency Detector (PFD)/Charge-Pump(CP)
  - Loop Filter (LF)
  - Voltage Controlled Oscillator (VCO)
  - Frequency Divider (÷N)

Classical CP PLL Working Principal

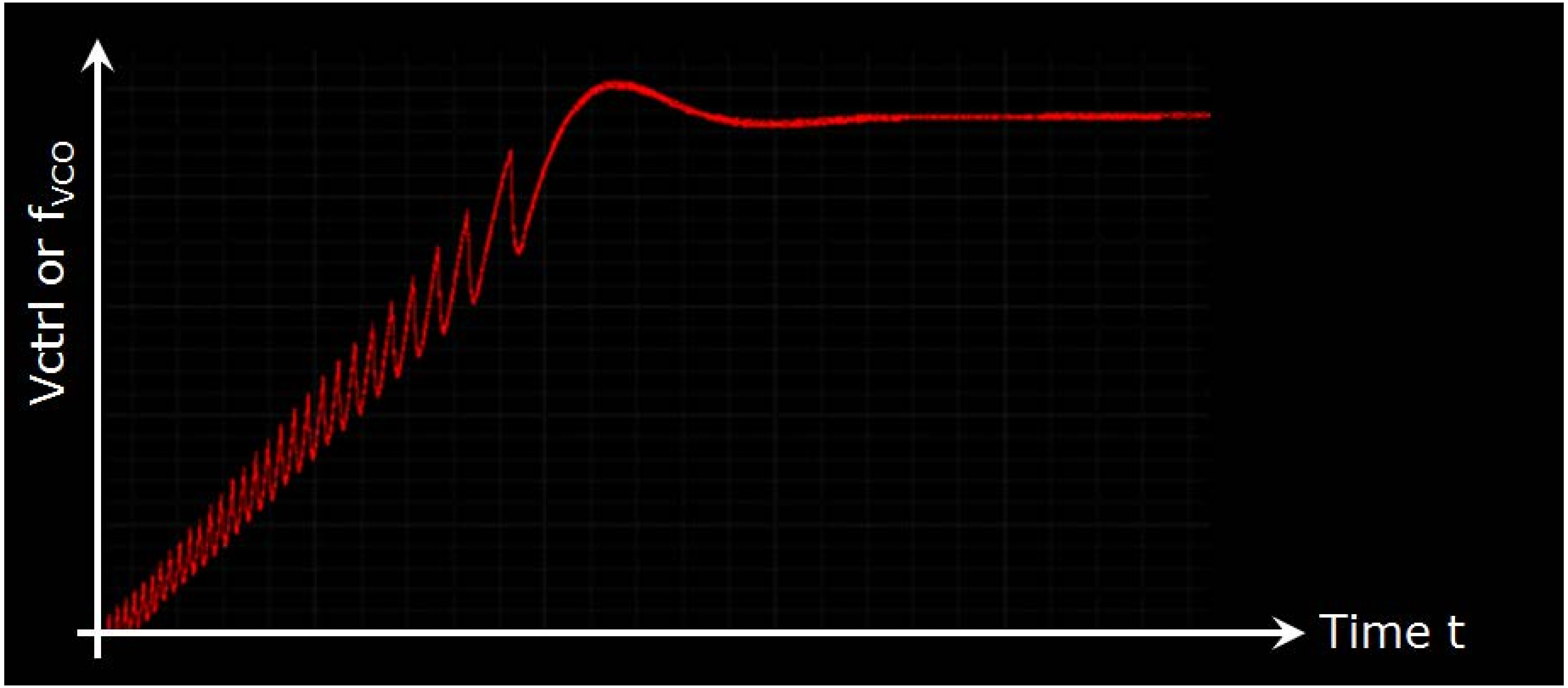




Phase Locked *VCO/Div* lags *VCO/Div* leads

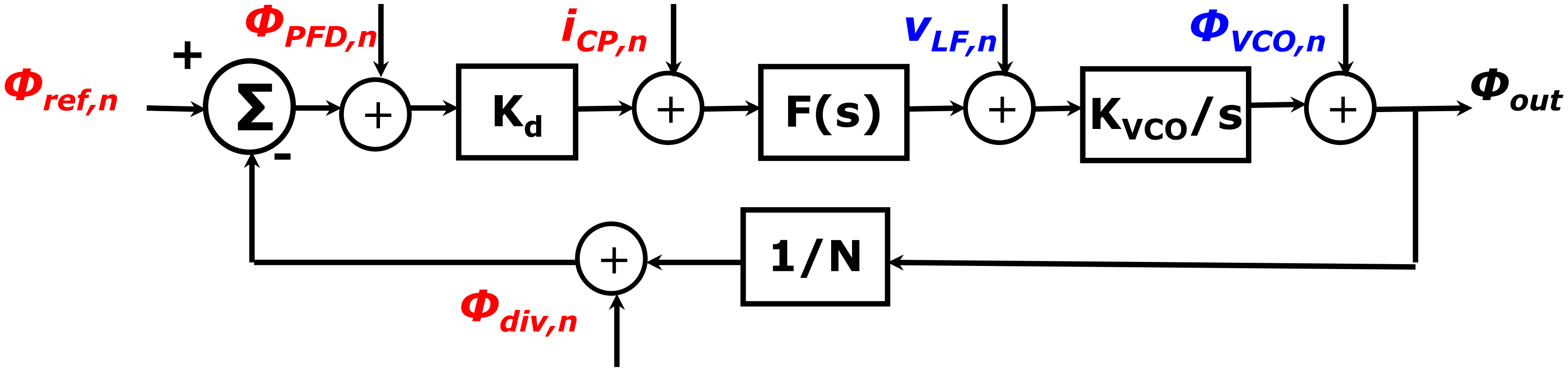
PLL Transient Response Example

- PLL transient response is generally a nonlinear process. The PLL operation is non-continuous (divider/PFD event driven, CP output non-continuous)



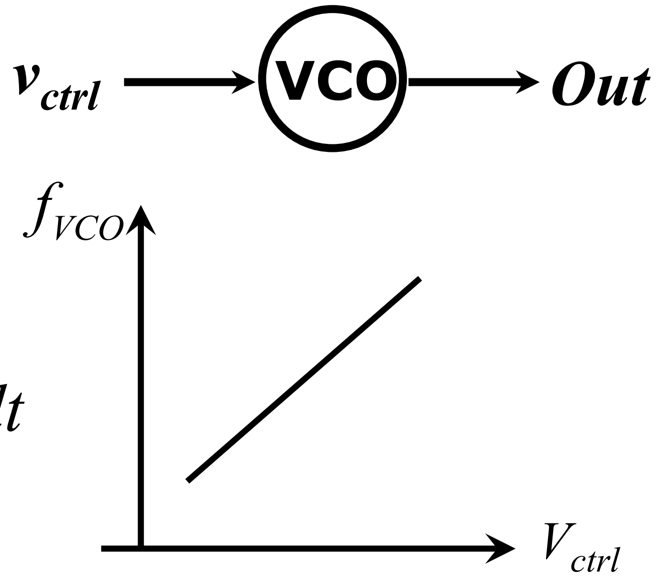
Linear Phase Domain Model

- However, once phase locked and if PLL bandwidth $f_c<f_{ref}/10$, a linear phase-domain model can be used for noise and stability analysis



- To analyze PLL phase noise, we can group the noise sources into two:
  - VCO noise: noise from LF/VCO/VCO buffer referred to VCO output
  - Non-VCO noise: noise from other loop components referred to PFD input, amplified by N^2 when referred to PLL output
- How do we derive this model?

VCO and Modeling



- VCO generates PLL output, its frequency and phase can be expressed as

$$\omega_{VCO} = \omega_{VCO,center} + v_{ctrl} \cdot K_{VCO}$$

$$\phi_{VCO}(t) = \int \omega_{VCO} dt = \int \omega_{VCO,center} \cdot dt + \int v_{ctrl} \cdot K_{VCO} \cdot dt$$

- Taking the Laplace transform (first term is a constant)

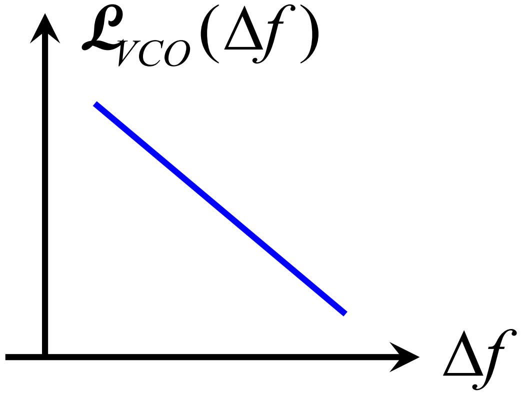
$$\phi_{VCO}(s) = v_{ctrl}(s) \frac{K_{VCO}}{s} \quad \Rightarrow \quad \frac{\phi_{VCO}(s)}{v_{ctrl}(s)} = \frac{K_{VCO}}{s}$$

- VCO in phase domain is an integrator

VCO Phase Noise

- VCO phase noise is fundamentally related to design parameters like oscillation frequency f_{VCO}, and power dissipation $P_{VCO.}$ The quality of a VCO design can be benchmarked using the classic VCO Figure-Of-Merit (FOM) [1]

$$FOM_{VCO} = 10\log\left(\mathcal{L}_{VCO}(\Delta f)\cdot\frac{\Delta f^2}{f_{VCO}^2}\cdot\frac{P_{VCO}}{1mW}\right)$$



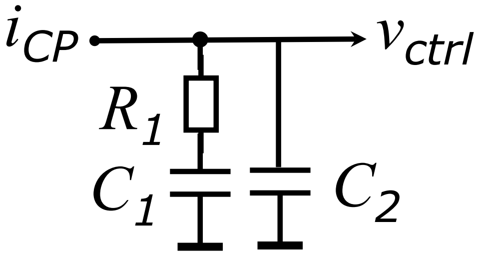
- Therefore, $$\mathcal{L}_{VCO}(\Delta f) = \frac{10^{FOM_{VCO}/10}}{P_{VCO}/1mW}\cdot\frac{f_{VCO}^2}{\Delta f^2}$$

- State-of-art VCO design’s FOM is <-190dBc/Hz, meaning e.g. <-130dBc/Hz phase noise at 1MHz offset at 1GHz output given 1mW power

Loop Filter and Noise

- The most common LF is a second order filter:

$$F_{LF}(s) = \frac{1}{s(C_1 + C_2)} \cdot \frac{sR_1C_1 + 1}{sR_1 \dfrac{C_1C_2}{C_1 + C_2} + 1}$$

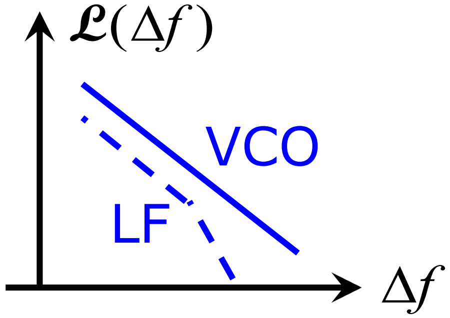


- LF noise is from the resistor R, referred to VCO output (assume $C_1 >> C_2$):

$$\mathcal{L}_{VCO-LF}(\Delta f) \approx \frac{1}{2} \times 4kTR_1 \times \left|\frac{1}{1 + sR_1C_2}\right|^2 \times \left|\frac{K_{VCO}}{s}\right|^2 \quad \text{with } s = j2\pi\Delta f$$

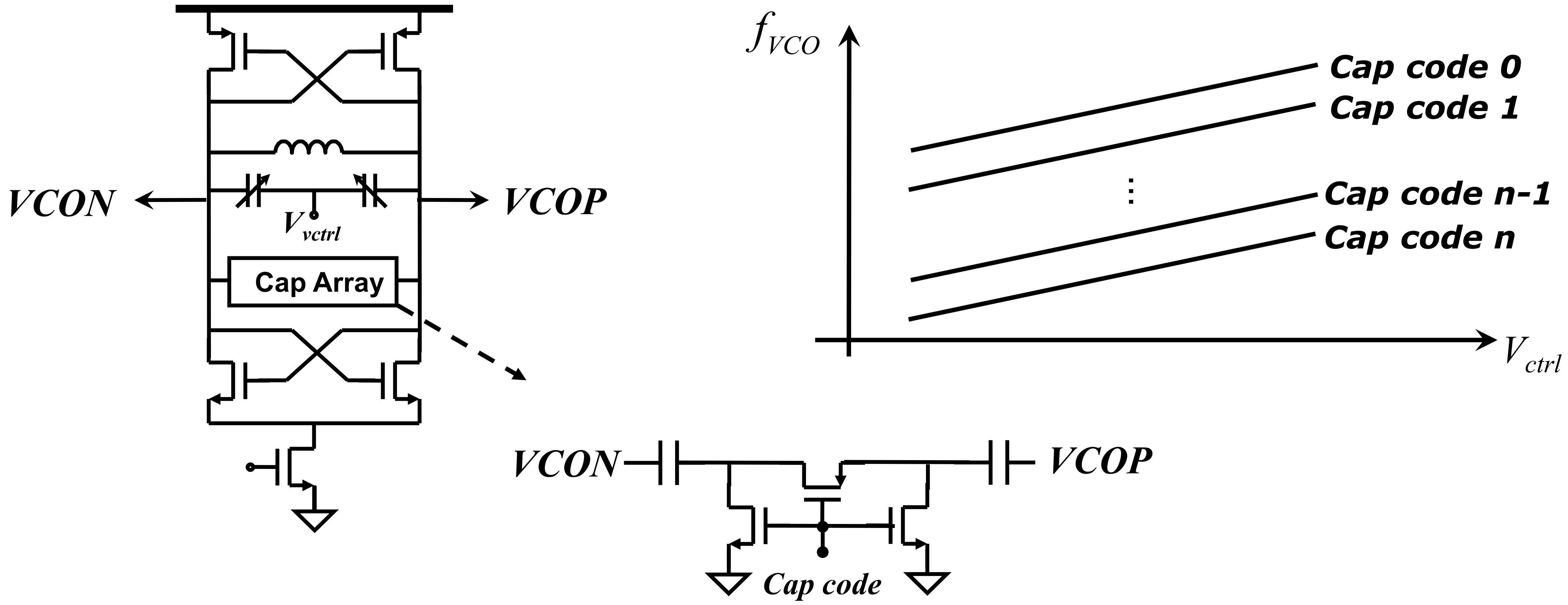
at small Δf :

$$\mathcal{L}_{VCO-LF}(\Delta f) \approx \frac{kT}{2\pi^2} \cdot R_1 \cdot K_{VCO}^2 \cdot \frac{1}{\Delta f^2}$$



- Targeting for low jitter and low power, LF noise should be made negligible compared with intrinsic VCO noise by reducing R_1 (at the expense of larger C) or reducing K_{VCO}

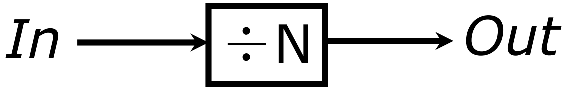
Typical VCO design



- Digital controlled coarse tuning cap to handle large tuning range requirement while keeping K_{VCO} low

Divider Modelling

- Basic function of a frequency divider $\omega_{out} = \frac{\omega_{in}}{N}$



- What's the effect of divider on phase modulated incoming signal?

  - Input phase $\phi_{in}(t) = \omega_{in}t + A_m \sin\omega_m t$

  - Instantaneous input frequency $\omega_{in,inst}(t) = \frac{d\phi_{in}(t)}{dt} = \omega_{in} + A_m\omega_m \cos\omega_m t$

  - Instantaneous output frequency $\omega_{out,inst}(t) = \frac{\omega_{in,inst}}{N} = \frac{\omega_{in}}{N} + \frac{A_m\omega_m \cos\omega_m t}{N}$

Divider Modelling, Cont'd

- The phase at divider output is

$$\phi_{out}(t) = \int \omega_{out,inst}(t) \cdot dt$$

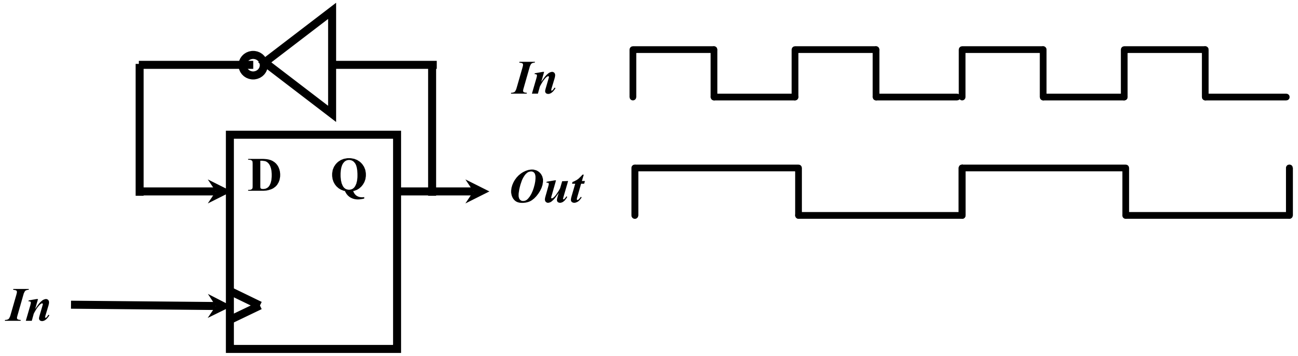
$$= \int \left(\frac{\omega_{in}}{N} + \frac{A_m \omega_m \cos \omega_m t}{N}\right) \cdot dt$$

$$= \frac{\omega_{in}}{N} t + \frac{A_m}{N} \sin \omega_m t$$

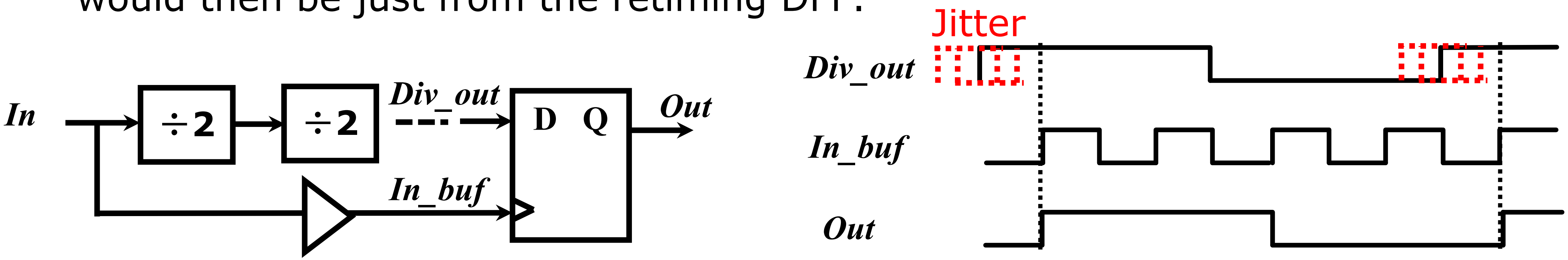
- For the modulated term, peak phase deviation is reduced by N. However, the modulation frequency is not affected.
- In phase domain, divider can thus be modeled as 1/N

Low Noise Divider Design

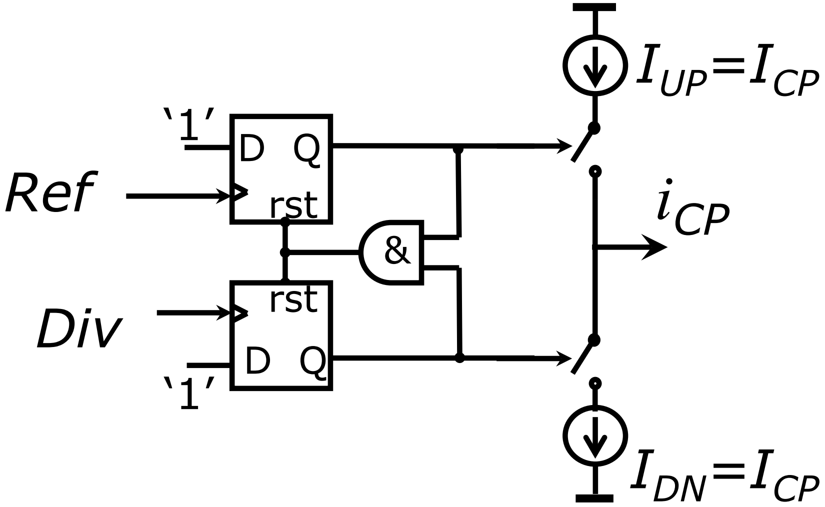
- Simple divide-by-2 design

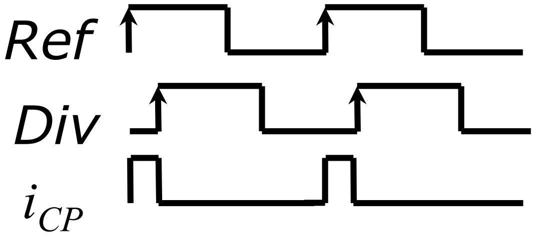


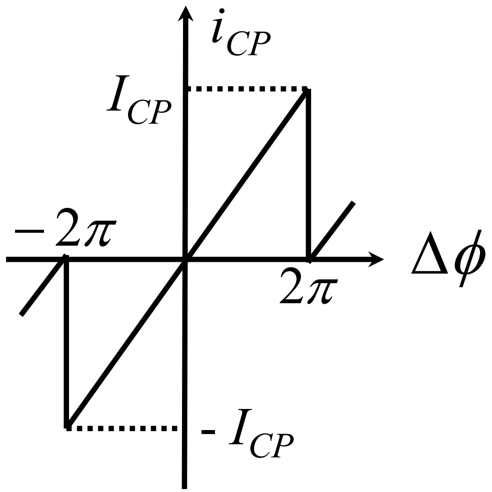
- If N is large, Div-N is often designed with multiple smaller divider stages in series, jitter accumulates over the stages
- Divider chain jitter can be removed using retimer at divider output. The jitter would then be just from the retiming DFF.



PFD/CP Modelling







- PFD detects timing error, the gain is $K_{PFD}=\frac{\Delta\varphi_{PFD-out}}{\Delta\varphi_{PFD-in}}=\frac{2\pi\times\Delta t/T_{ref}}{2\pi\times\Delta t/T_{ref}}=1$
- CP pumps current into LF, the gain is

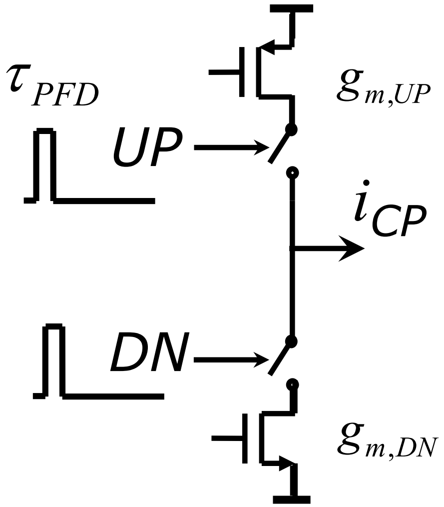
$$K_{CP}=\frac{\overline{i_{CP}}}{\Delta\phi_{PFD-out}}=\frac{I_{CP}\times\Delta t/T_{ref}}{2\pi\times\Delta t/T_{ref}}=\frac{I_{CP}}{2\pi}\quad \text{thus}\quad K_d=K_{PFD}\cdot K_{CP}=\frac{I_{CP}}{2\pi}$$

CP Noise

- Assume the simplest CP design and same UP/DN transistor gm, the PSD of the CP thermal noise current is

$$S_{iCP,n}(f) = 4kT\gamma \cdot (g_{m,UP} + g_{m,DN})$$

$$\approx 8kT\gamma \cdot (2I_{CP} / V_{eff,CP})$$



$$g_{m,UP} = \frac{2I_{CP}}{V_{gs} - V_{th}} = \frac{2I_{CP}}{V_{eff,CP}}$$

$$g_{m,DN} = g_{m,UP}$$

- In steady state, CP is switched on only for a fraction of time τ_{PFD} of each period T_{ref} to avoid the CP dead zone. The equivalent CP noise is:

$$S_{iCP,n}(f) = 16kT\gamma \cdot \frac{I_{CP}}{V_{eff,CP}} \cdot \frac{\tau_{PFD}}{T_{ref}}$$

- The theoretical minimum power needed by a CP is: $P_{CP} = I_{CP} V_{DD} \times \frac{\tau_{PFD}}{T_{ref}}$

CP Noise Referred to PLL Output

- CP noise referred to PLL output

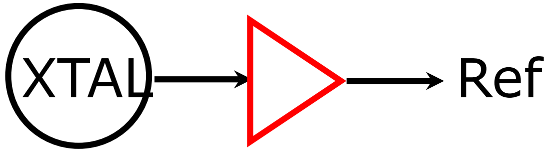
$$\mathcal{L}_{PLL-CP}(\Delta f) = \frac{S_{iCP,n}(f)/2}{(\frac{I_{CP}}{2\pi}\cdot\frac{1}{N})^2} = \frac{f_{out}^2}{f_{ref}}\cdot\frac{32\pi^2 kT\gamma}{V_{eff,CP}}\cdot\frac{1}{I_{CP}}\cdot\frac{\tau_{PFD}}{T_{ref}}$$

$$\Rightarrow \qquad \mathcal{L}_{PLL-CP}(\Delta f) = \frac{f_{out}^2}{P_{CP}}\cdot\{\tau_{PFD}^2\cdot\frac{32\pi^2\gamma\cdot kT\cdot V_{DD}}{V_{eff,CP}}\}$$

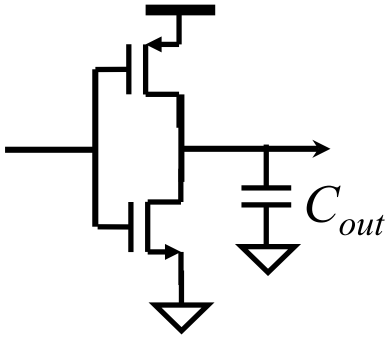
- To minimize CP noise, designer should maximize the CP current source over-drive voltage, minimize switch-on time, or burn more power with larger I_{CP}

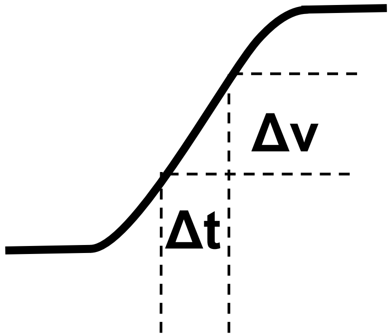
Reference Noise

- Reference clock is often provided by an off-chip clock source like a XTAL oscillator. On chip clock buffers adds jitter to it.



- Jitter generated by a simple inverter buffer can be related to the rms voltage noise and slew rate SR_{out} at inverter output [2]:

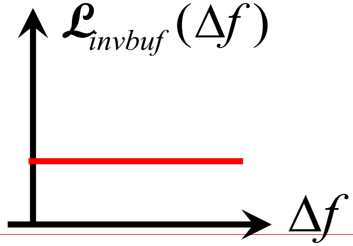




$$\sigma_{t,invbuf}^2 = \frac{F_n \cdot kT / C_{out}}{SR_{out}^2}$$

F_n : excess noise factor

- For thermal noise, PSD is white:



$$\sigma_{t,invbuf}^2 = \frac{2 \times \int_0^{f_{ref}/2} \mathcal{L}_{invbuf}(\Delta f) df}{(2\pi f_{ref})^2} \Rightarrow \mathcal{L}_{invbuf}(\Delta f) = 4\pi^2 \cdot f_{ref} \cdot \frac{F_n \cdot kT / C_{out}}{SR_{out}^2}$$

Inverter Clock Buffer Noise

- When referred to PLL output:

$$\mathcal{L}_{PLL-invbuf}(\Delta f) = N^2 \cdot \mathcal{L}_{invbuf}(\Delta f) = \frac{f_{out}^2}{f_{ref}} \cdot 4\pi^2 \cdot \frac{F_n \cdot kT / C_{out}}{SR_{out}^2}$$

- On the other hand, theoretical minimum inverter power is dynamic power:

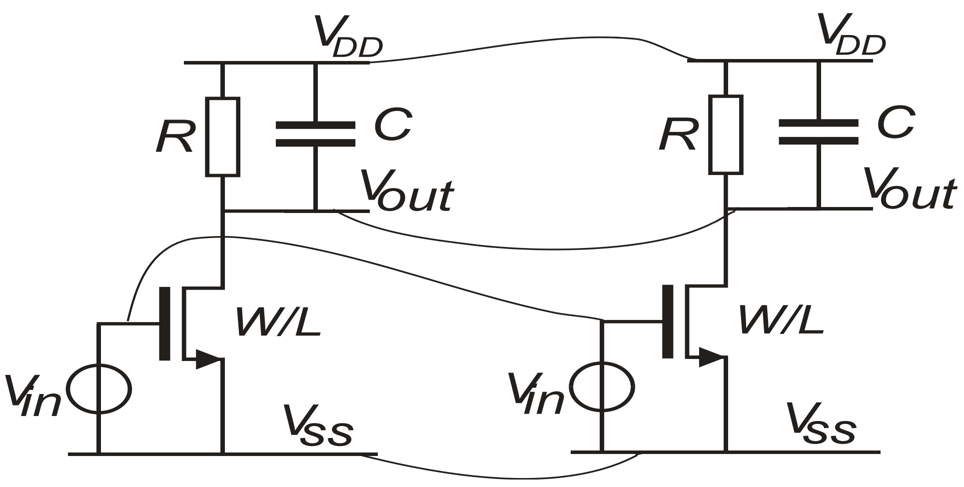
$$P_{invbuf} = f_{ref} \cdot C_{tot} \cdot V_{DD}^2$$

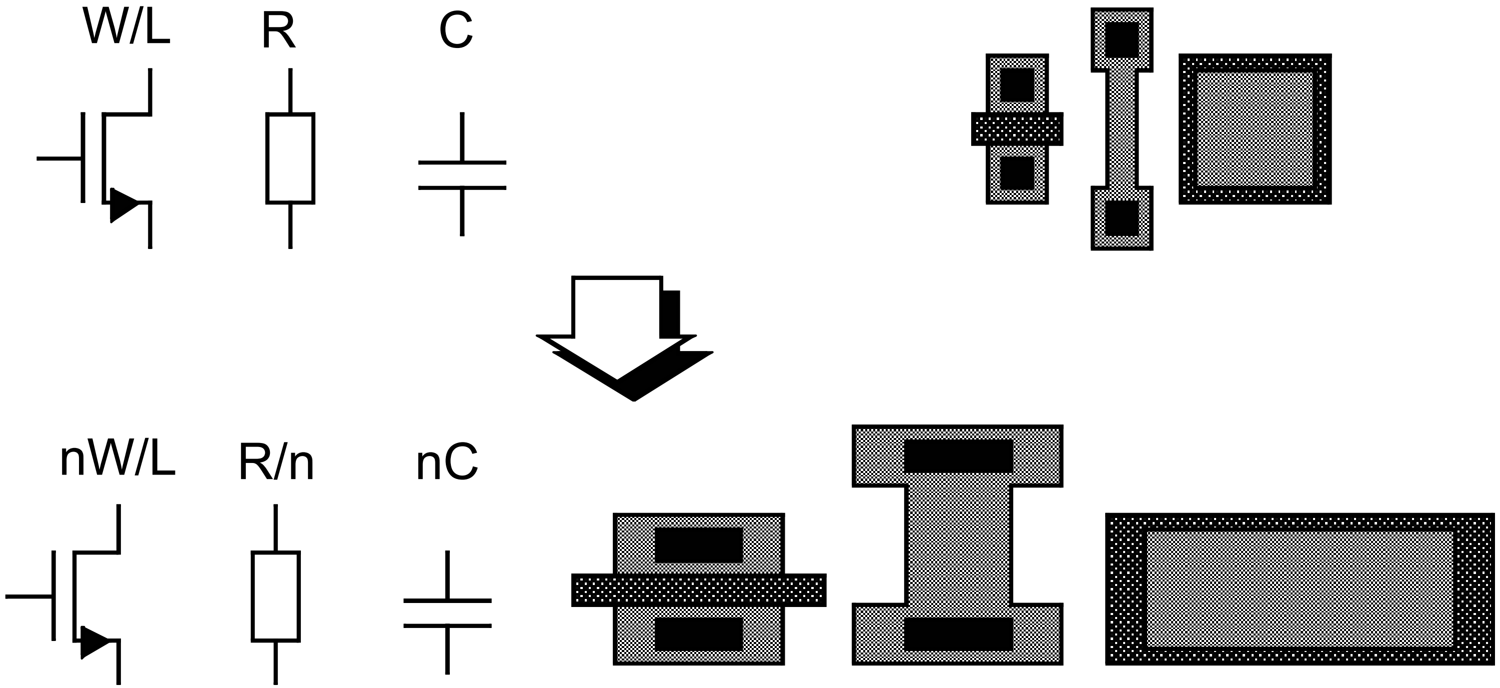
$$\Rightarrow \mathcal{L}_{PLL-invbuf}(\Delta f) = \frac{f_{out}^2}{P_{invbuf}} \cdot \{\frac{4\pi^2 \cdot F_n \cdot kT \cdot V_{DD}^2}{SR_{out}^2} \cdot \frac{C_{tot}}{C_{out}}\}$$

- To minimize inverter buffer noise, designer should maximize output slew rate, minimize noise factor and C_{tot}/C_{out} . For further lower noise, burn more power.
- Similar analysis applies to other event driven circuits e.g. DFFs in divider/PFD

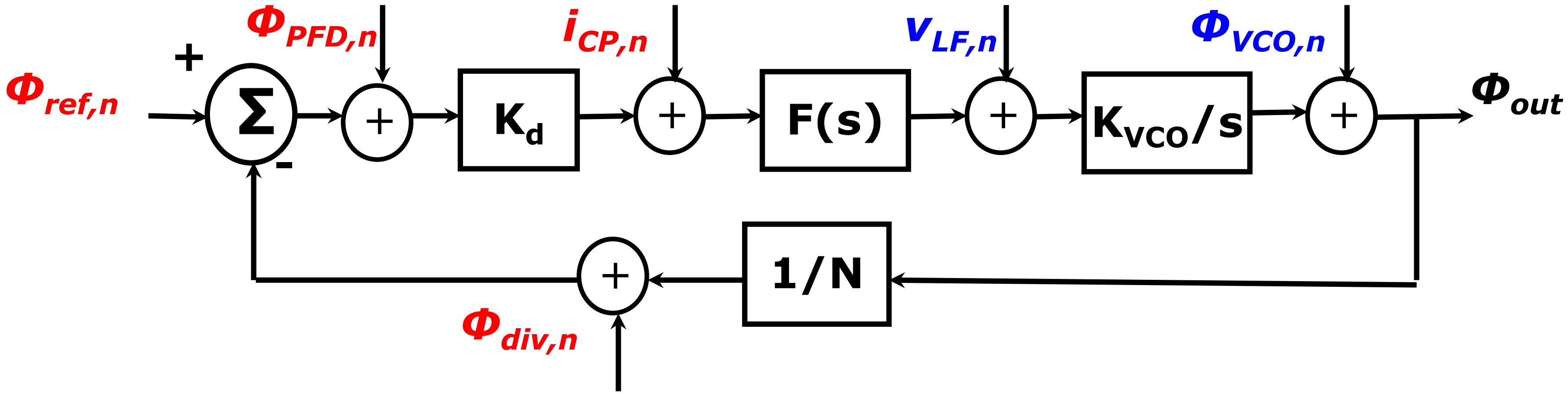
Burn More Power (Impedance Level Scaling)

- Put two identical circuit in parallel and connect all the nodes, power and area would double but noise will be reduced by 3dB





Linear Phase Domain Model With Noise



- Now we know the PLL open loop gain is

$$G(s) = \frac{1}{N} \cdot \frac{I_{CP}}{2\pi} \cdot \frac{1}{s(C_1 + C_2)} \cdot \frac{sR_1C_1 + 1}{sR_1 \dfrac{C_1C_2}{C_1 + C_2} + 1} \cdot \frac{K_{VCO}}{s}$$

- This is a 3rd order type-II PLL (two poles at origin)

PLL Open Loop Gain and Bode Plot

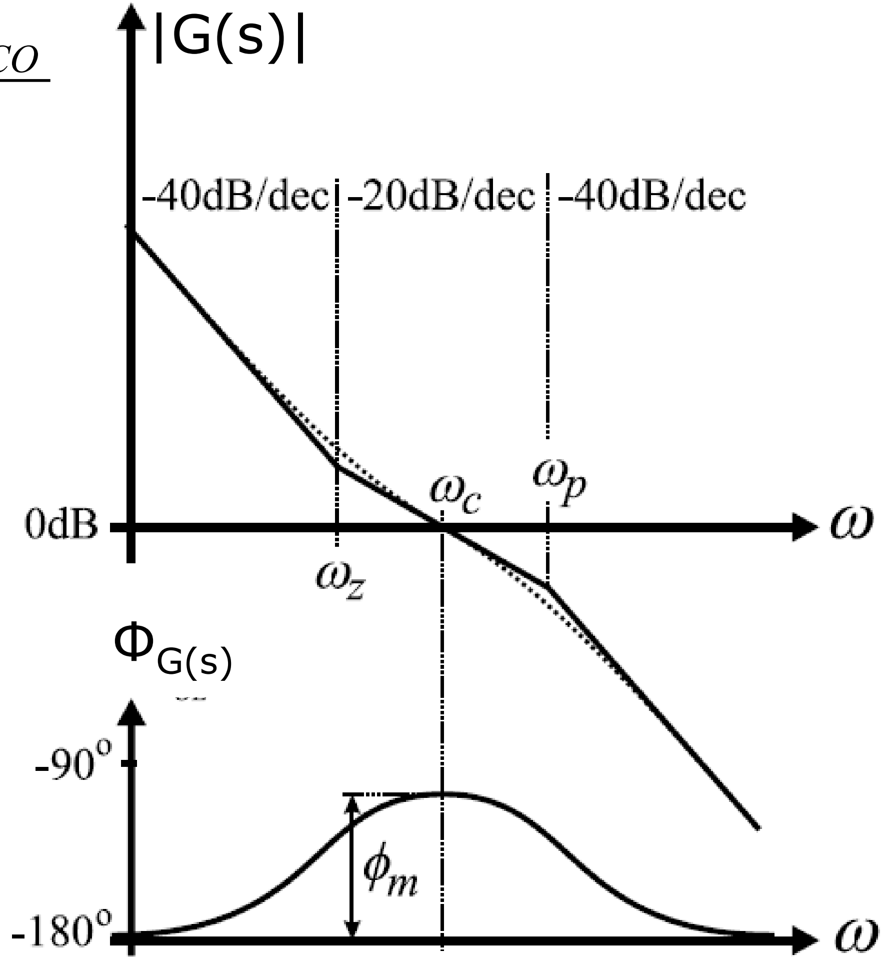
$$G(s)=\frac{1}{N}\cdot\frac{I_{CP}}{2\pi}\cdot\frac{1}{s(C_1+C_2)}\cdot\frac{sR_1C_1+1}{sR_1\dfrac{C_1C_2}{C_1+C_2}+1}\cdot\frac{K_{VCO}}{s}$$

$$\omega_z=\frac{1}{R_1C_1}\qquad \omega_p=\frac{1}{R_1\dfrac{C_1C_2}{C_1+C_2}}$$

$$\omega_c\approx\frac{I_{CP}\cdot R_1\cdot K_{VCO}}{2\pi\cdot N}$$ (assume $C_1>>C_2$)

$$\phi_m=\arctan\frac{\omega_c}{\omega_z}-\arctan\frac{\omega_c}{\omega_p}$$

- E.g., $\omega_c/\omega_z=4$, $\omega_c/\omega_p=1/4$, phase margin is about 62 degree



PLL Noise Transfer Function

- Noise transfer function from VCO to PLL output

$$H_{VCO}(s) = \frac{1}{1 + \frac{1}{N} \cdot K_d \cdot F_{LF}(s) \cdot \frac{K_{VCO}}{s}} = \frac{1}{1 + G(s)}$$

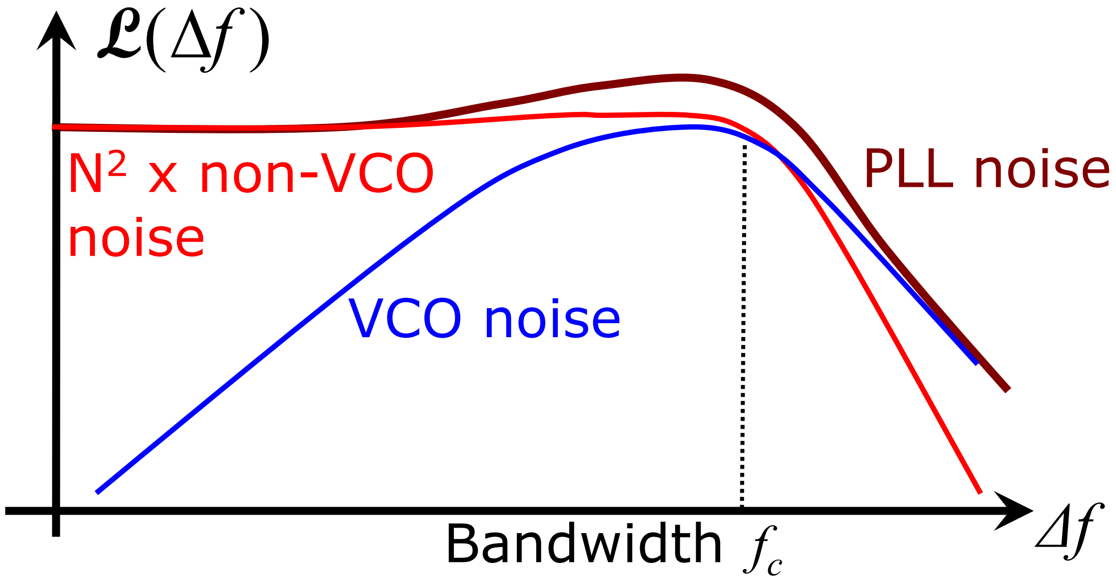
High pass filtered

- Noise transfer function from (PFD input referred) non-VCO noise to PLL output

$$H_{non-VCO}(s) = N \cdot \frac{G(s)}{1 + G(s)} = N \cdot [1 - H_{VCO}(s)]$$

Low pass filtered, amplified by N

Overall PLL Phase Noise and Jitter



$$\sigma^2_{t,non-VCO} = \frac{2\int_{f_L}^{f_H} \mathcal{L}_{non-VCO}(\Delta f)\,|H_{non-VCO}(j2\pi\Delta f)|^2\,df}{(2\pi f_{out})^2}$$

$$\sigma^2_{t,VCO} = \frac{2\int_{f_L}^{f_H} \mathcal{L}_{VCO}(\Delta f)\,|H_{VCO}(j2\pi\Delta f)|^2\,df}{(2\pi f_{out})^2}$$

$$\sigma^2_{t,PLL} = \frac{2\int_{f_L}^{f_H} \mathcal{L}_{PLL}(\Delta f)\,df}{(2\pi f_{out})^2} = \sigma^2_{t,VCO} + \sigma^2_{t,non-VCO}$$

- Non-VCO noise low pass filtered dominates in-band, VCO noise high pass filtered dominates out-band, thus involve bandwidth tradeoff
- Optimum bandwidth $f_{c,opt}$ is approximately where VCO and non-VCO noise intersects. At $f_{c,opt}$, VCO and non-VCO components contribute equal jitter [3]

PLL FOM

- In an optimized PLL, VCO and non-VCO components not only contributes equally to jitter, but also equally to power [3]. Once optimization is done, the fundamental way to improve jitter is to burn more power

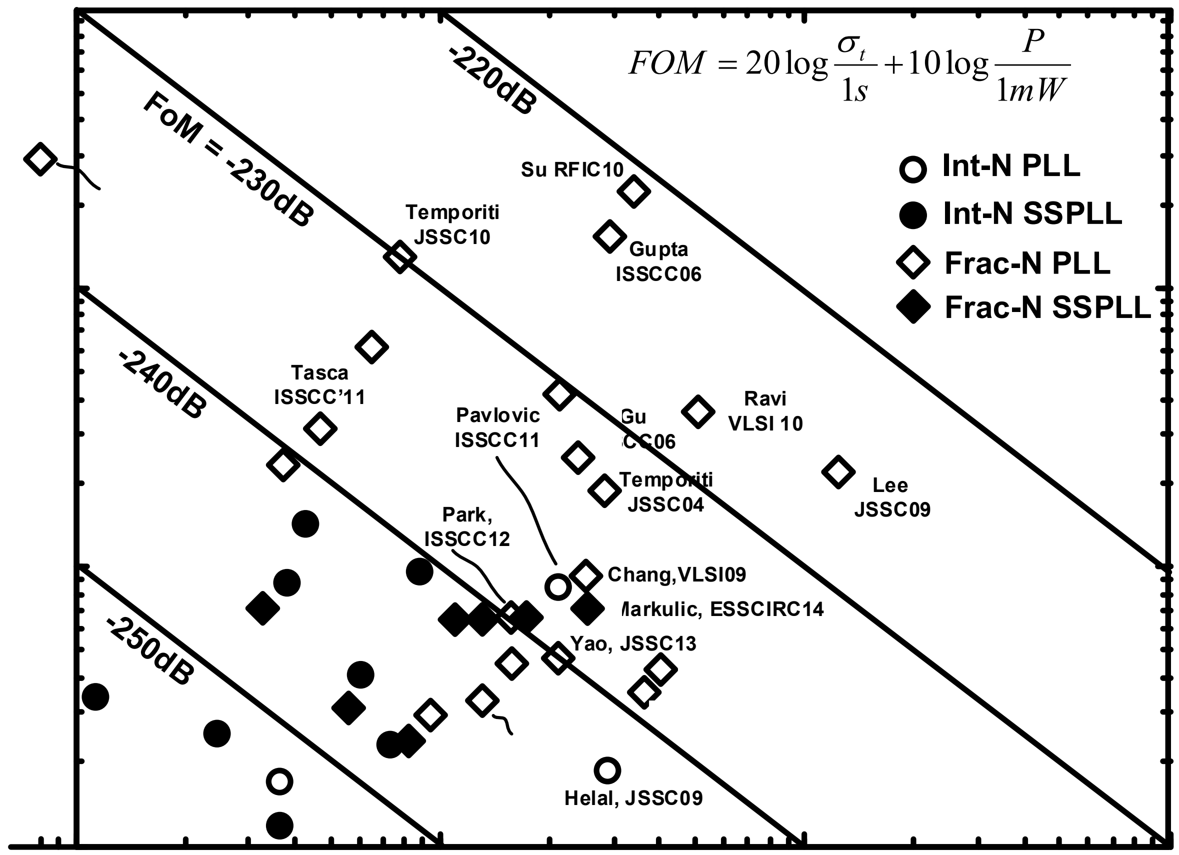
$$\sigma^2_{t,PLL} \propto \frac{1}{P_{PLL}}$$

- A PLL benchmarking FOM can thus be defined as

$$FOM_{PLL} = 10\log[(\frac{\sigma_{t,PLL}}{1s})^2 \cdot \frac{P_{PLL}}{1mW}]$$

- The design quality of VCO and non-VCO components are equally important in achieving good PLL FOM

State-of-Art PLL FOMs



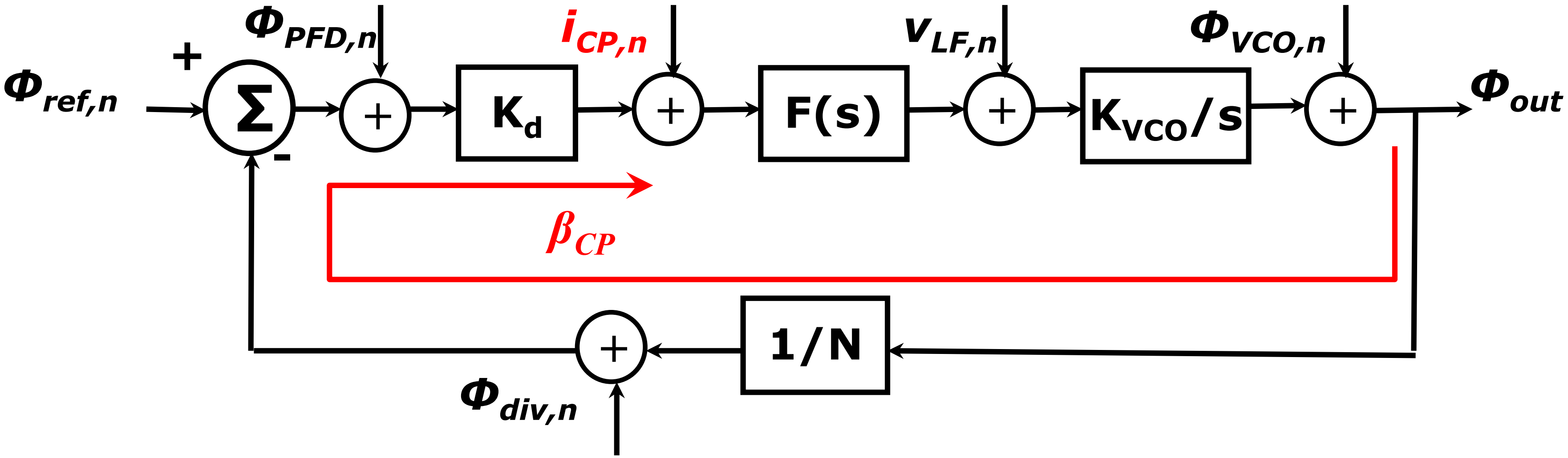
- PLL FOM improves over the years, Sub-Sampling PLLs achieved state-of-art FOM

Outline

- PLL Basics
- Classical CP PLL Analysis and Optimization
- **Low Jitter Sub-Sampling PLL Architecture**
- Frac-N Sub-Sampling PLL
- Conclusion

CP Noise and CP Feedback Gain

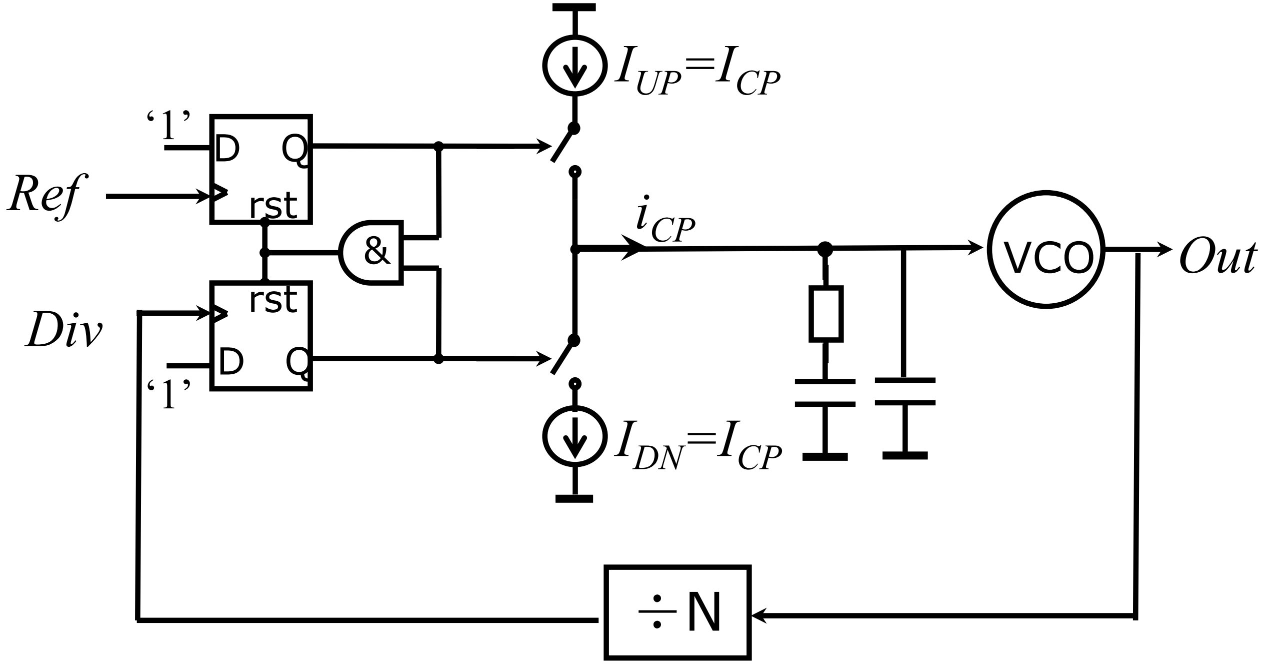
- CP is one of the major PLL noise source



- Define CP feedback gain β_{CP} , $\mathcal{L}_{PLL-CP}(\Delta f) = \dfrac{S_{iCP,n}(f)/2}{(\beta_{CP})^2}$

- CP noise is suppressed by β_{CP} , large β_{CP} desired for low noise

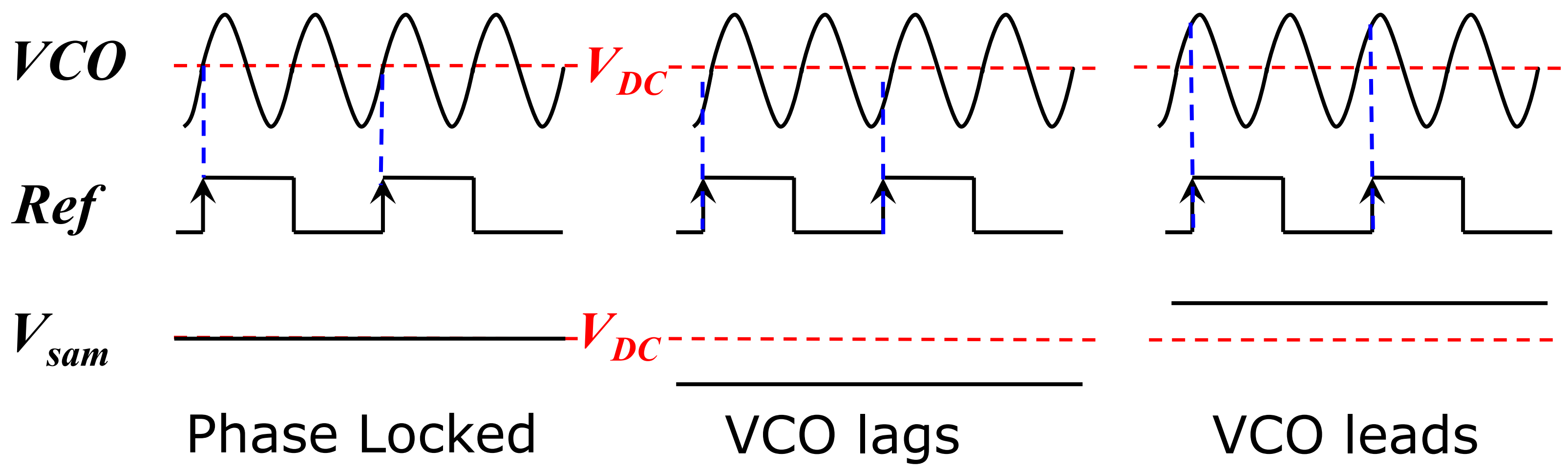
Classical PLL CP Feedback Gain



- β_{CP} reduced by N, thus CP noise amplified by N^2

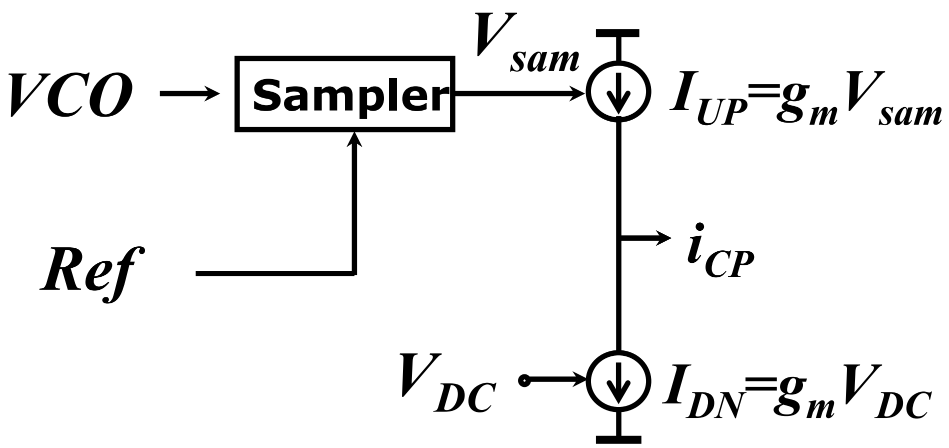
$$\beta_{CP,class} = \boxed{\frac{1}{N}} \times \frac{I_{CP}}{2\pi}$$

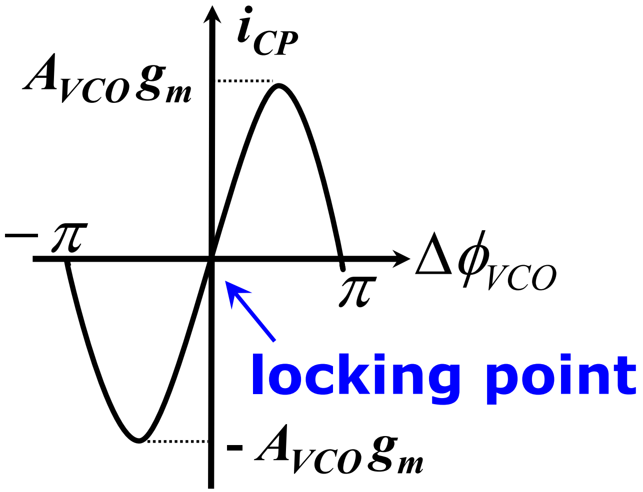
Sub-Sampling Phase Detector (SSPD)



- Sub-Sampling PD for Integer-N PLL [4]
  - VCO sub-sampled by Ref without going through divider
  - Phase/Timing error converted into voltage error
  - High phase detection gain due to high VCO slew rate (dv/dt)

Sub-Sampling PD/CP (SSPD/CP)





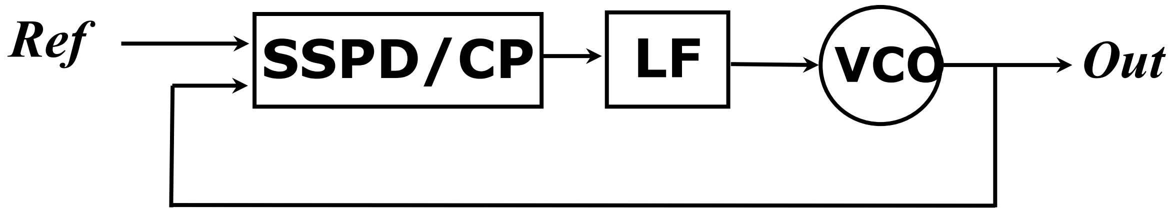
- Voltage controlled CP
- Ideal characteristic

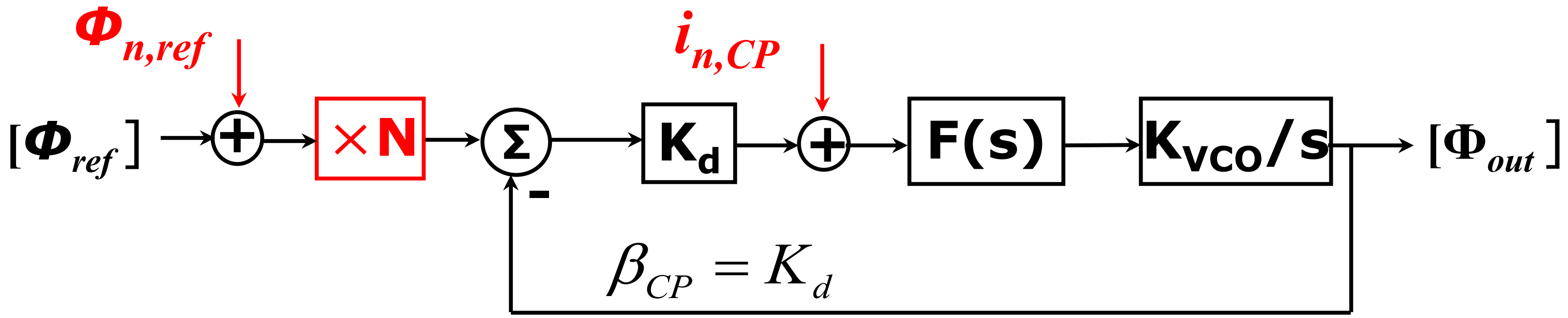
- Detection characteristic is fairly linear once in lock

$$\beta_{CP,SS} = \frac{\overline{i_{CP}}}{\Delta\phi_{VCO}} = \frac{A_{VCO}\sin(\Delta\phi_{VCO}) \cdot g_m}{\Delta\phi_{VCO}} \approx A_{VCO} \cdot g_m$$

There is no N factor

SSPLL and Modeling

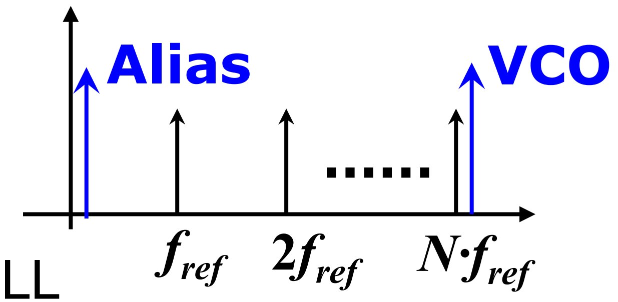




- No Divider but a virtual Multiplier
  - Sub-sampling process

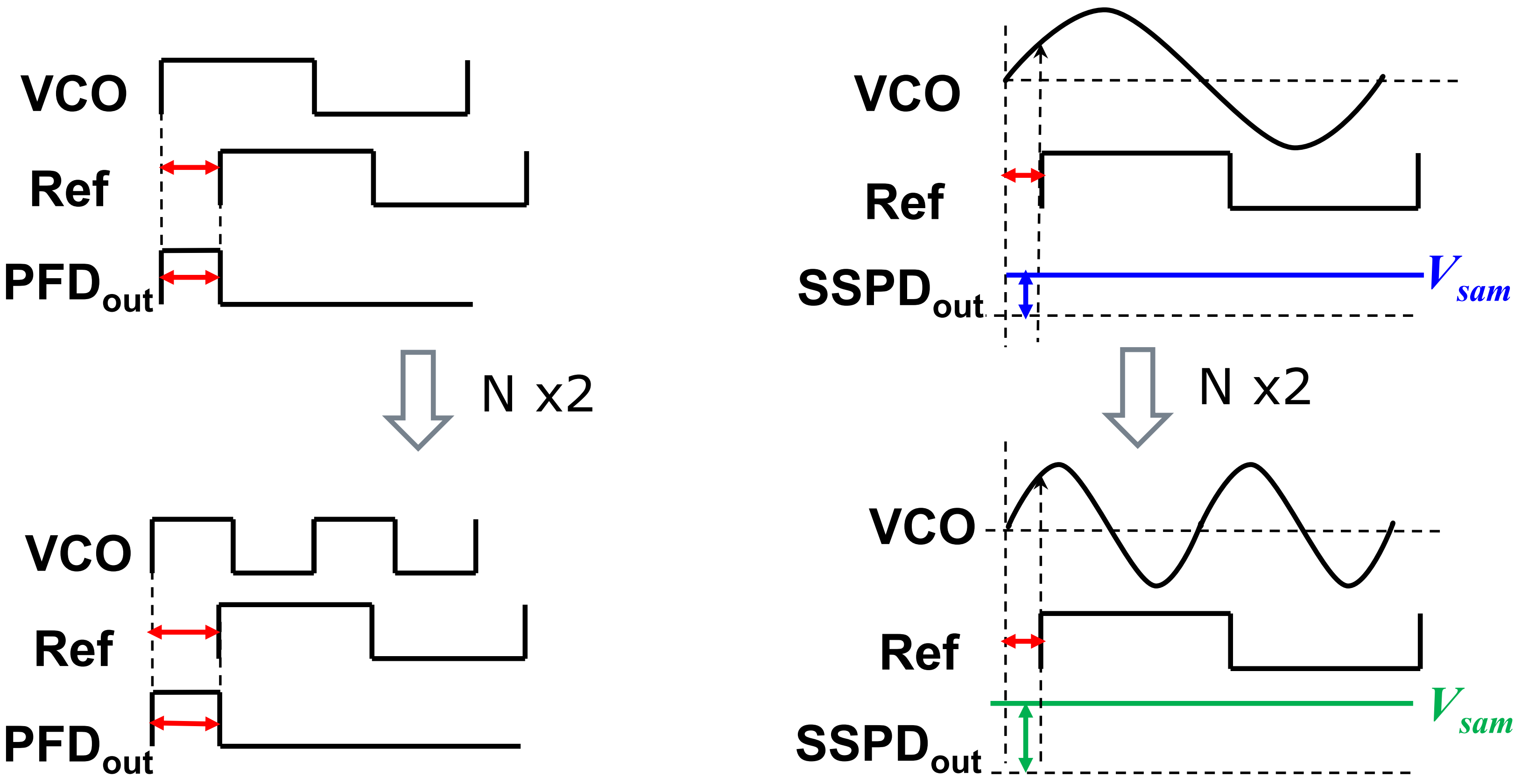
$$f_{alias} = f_{VCO} - N \cdot f_{ref}$$

  - Ref noise multiplied by N^2, same as classical PLL



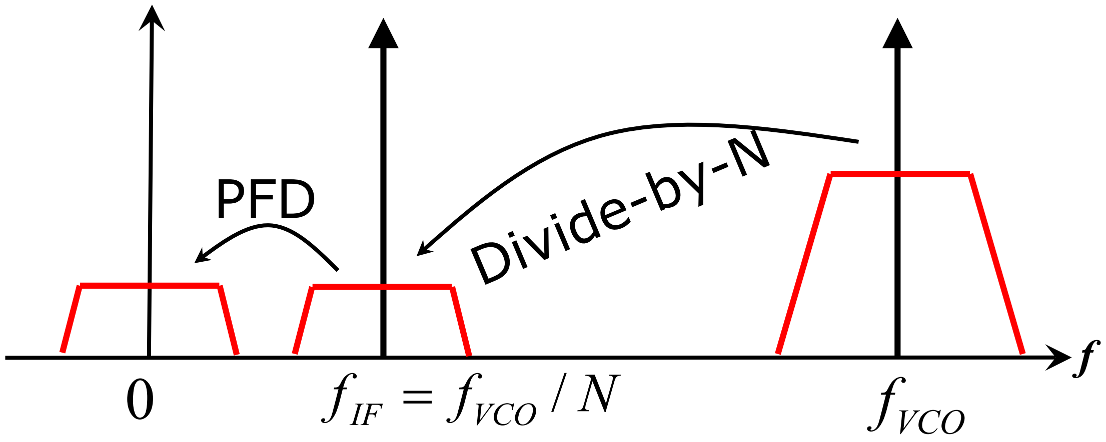
CP noise *not* multiplied by N^2

Essential Difference In Phase Detection



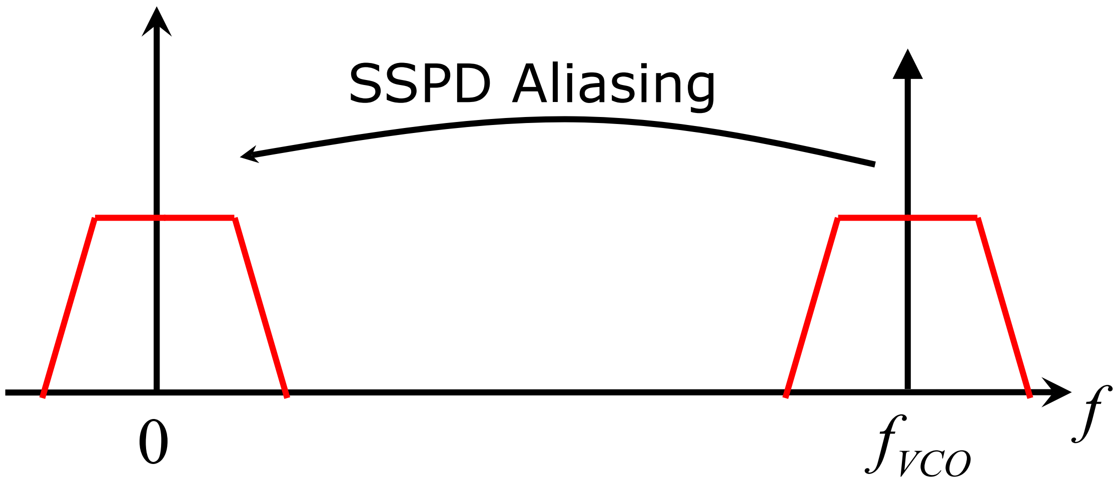
- Same PD output, thus β_{CP} halved acts as Δt detector
- PD output x2 (SlewRate x2), thus same β_{CP} acts as Δϕ detector

N Factor On CP Noise: Another Angle



- PLL is a loop back transceiver: VCO transmits 'signal' (VCO noise), the Loop receive/process it and feed it back to cancel/suppress the VCO noise
- Classical PLL is similar to a superheterodyne receiver
  - Divider: 1st down-converter, to low IF
  - PFD: 2nd down-converter, to DC
  - CP/LF: base band (TIA/LF)
- Divider as down-converter has 1/N attenuation, PFD/CP noise thus amplified by N^2

Why no N Factor In SSPLL



- SSPLL is similar to a direct conversion receiver
- SSPD down-converter has no attenuation but a gain of 1, thus no amplification for PD/CP noise

SSPLL VS Classical PLL

- SSPLL ideally has no divider noise
- SSPLL CP noise greatly suppressed by large β_{CP}
  - Comparing β_{CP} with classical PFD/CP assuming same I_{CP}

$$\frac{\beta_{CP,SSPD}}{\beta_{CP,PFD}} = \frac{A_{VCO} g_m}{(I_{CP}/2\pi)/N} = 4\pi \cdot N \cdot \frac{A_{VCO}}{2I_{CP}/g_m} = 4\pi \cdot N \cdot \frac{A_{VCO}}{V_{eff,CP}} >> 1$$

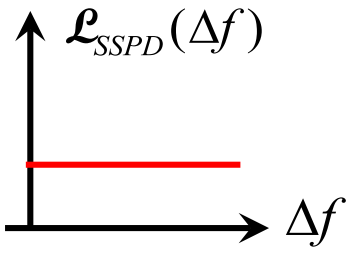
e.g. $= 4\pi \times 40 \times \frac{0.4V}{0.2V} \approx 1000$

SSPLL has much larger β_{CP}, thus more CP noise suppression

SSPD Noise

- The sampling process would add kT/C noise and cause jitter

$$\sigma_{t,SSPD}^2 = \frac{\overline{v_n^2}}{SR_{out}^2} = \frac{kT / C_{out}}{(A_{VCO} \cdot \omega_{VCO})^2}$$



- With white PSD, the SSPD phase noise is:

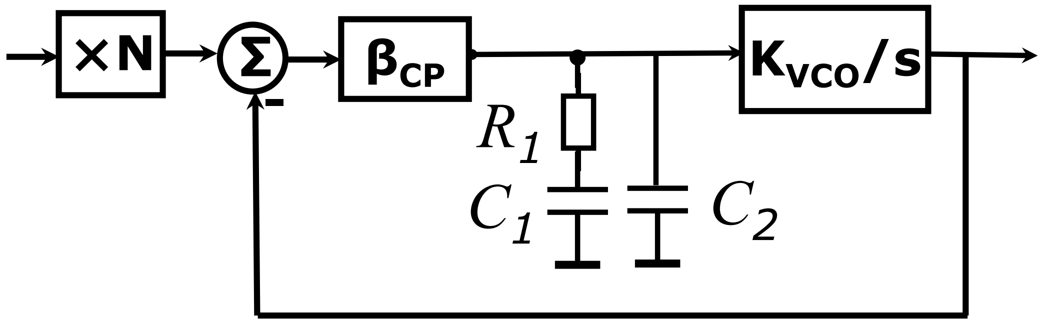
$$\sigma_{t,SSPD}^2 = \frac{2 \times \int_0^{f_{ref}/2} \mathcal{L}_{SSPD}(\Delta f) df}{(2\pi f_{ref})^2} \Rightarrow \mathcal{L}_{SSPD}(\Delta f) = \frac{kT}{C_{sam} \cdot f_{ref} \cdot A_{VCO}^2}$$

e.g. $= \frac{4 \times 10^{-21}}{10f \times 40M \times 0.4^2} \approx -132 dBc / Hz$

- 10fF C_{sam} enough for very low phase noise

SSPLL Design Challenges

- SSPLL has no divider, may lock to any integer N
- SSPD/CP has very large β_{CP} , may need big cap for stabilization



$$\omega_z = \frac{1}{R_1 C_1}$$

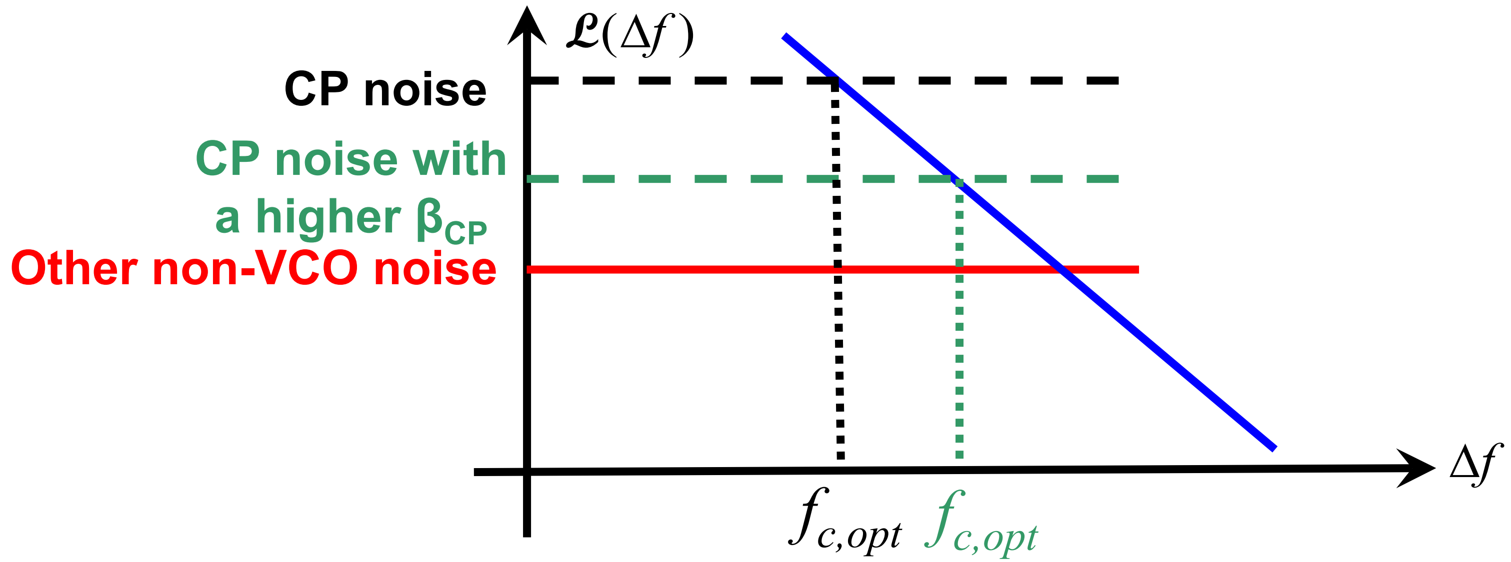
$$\omega_c \approx \beta_{CP} \cdot K_{VCO} \cdot R_1$$

$$C_1 \approx \{K_{VCO} \cdot \frac{\omega_c}{\omega_z}\} \cdot \frac{\beta_{CP}}{\omega_c^2}$$

- Once the design choice of K_{VCO} and ω_c / ω_z has been made

$$C_1 \propto \frac{\beta_{CP}}{\omega_c^2} \quad \text{or} \quad C_1 \propto \frac{\beta_{CP}}{f_c^2}$$

Relating β_{CP} , $f_{c,opt}$ and Filter Area

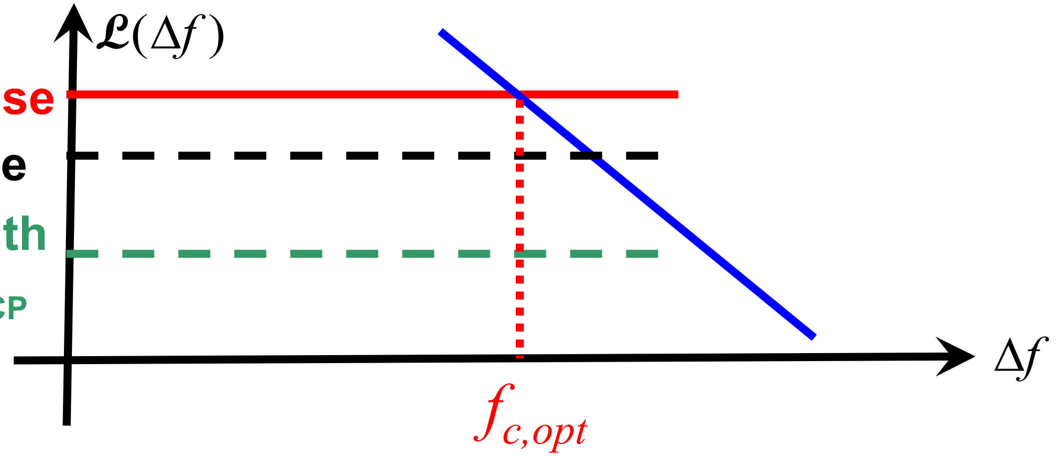


- When CP noise is much higher than other noise

$$\left.\begin{array}{l} f_{c,opt} \propto \beta_{CP} \\ C_1 \propto \dfrac{\beta_{CP}}{f_{c,opt}^2} \end{array}\right\} \quad C_1 \propto \frac{1}{\beta_{CP}}$$

Larger β_{CP} saves area

Relating β_{CP} , $f_{c,opt}$ and Filter Area



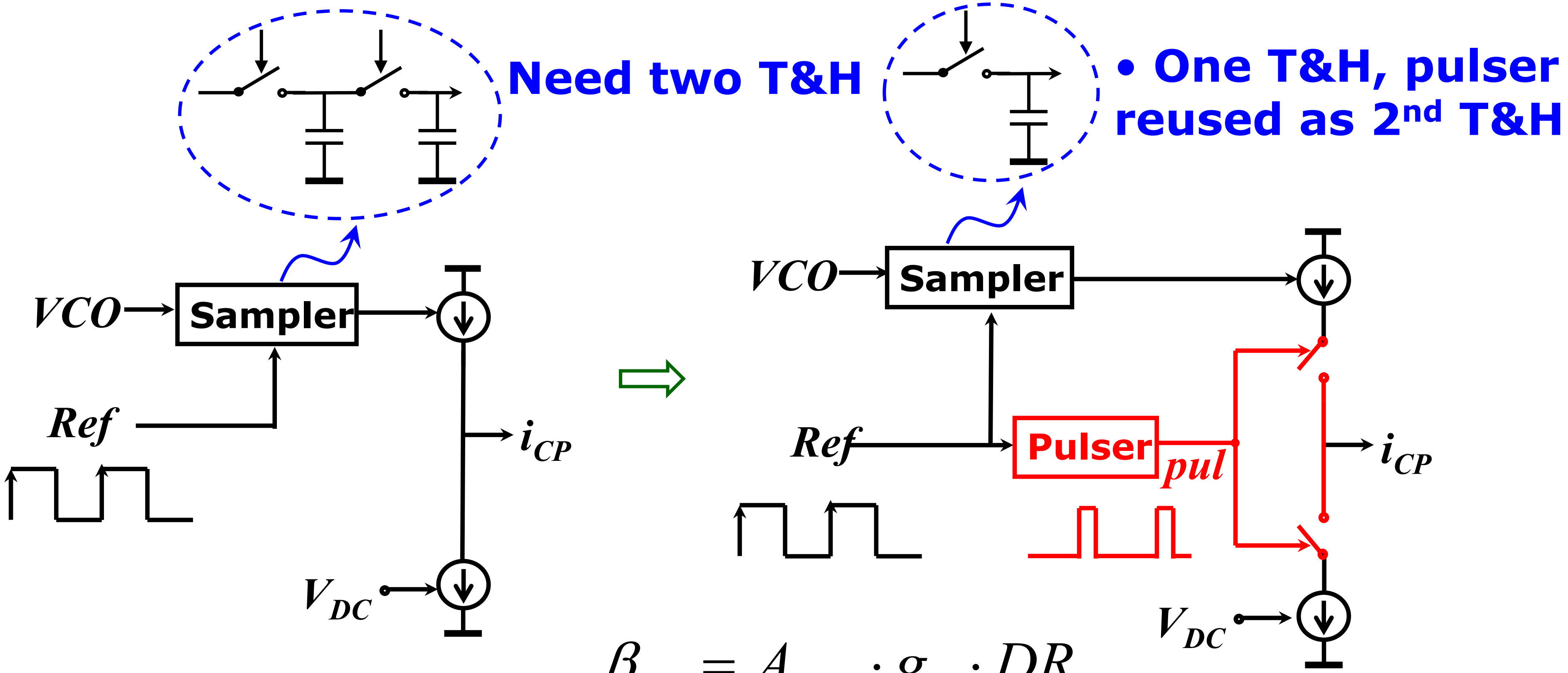
- When CP noise is no longer dominating loop noise,

$$\left.\begin{array}{l} f_{c,opt} = Const \\ C \propto \dfrac{\beta_{CP}}{f_{c,opt}^2} \end{array}\right\} \quad C \propto \beta_{CP}$$

Larger β_{CP} wastes area

- Once CP noise is negligible, further larger β_{CP} only wastes area

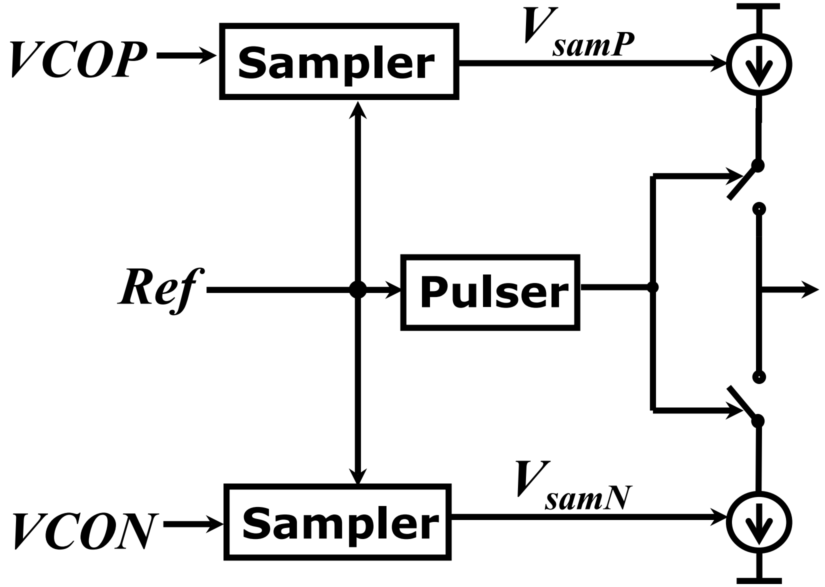
SSPD/CP with Gain Control

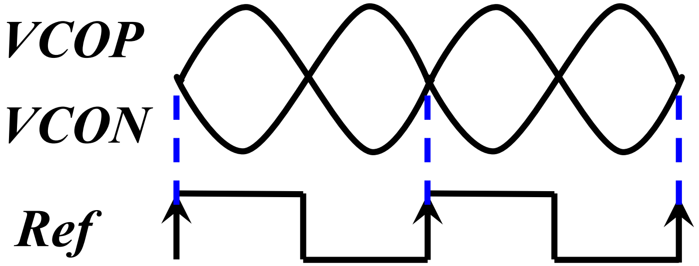


$$\beta_{CP} = A_{VCO} \cdot g_m \cdot DR_{pul}$$

- A proper choice of Pulser duty ratio DR_{pul} reduces filter area while keeping CP noise negligible. Pulser also reduces the sample and hold induced loop delay

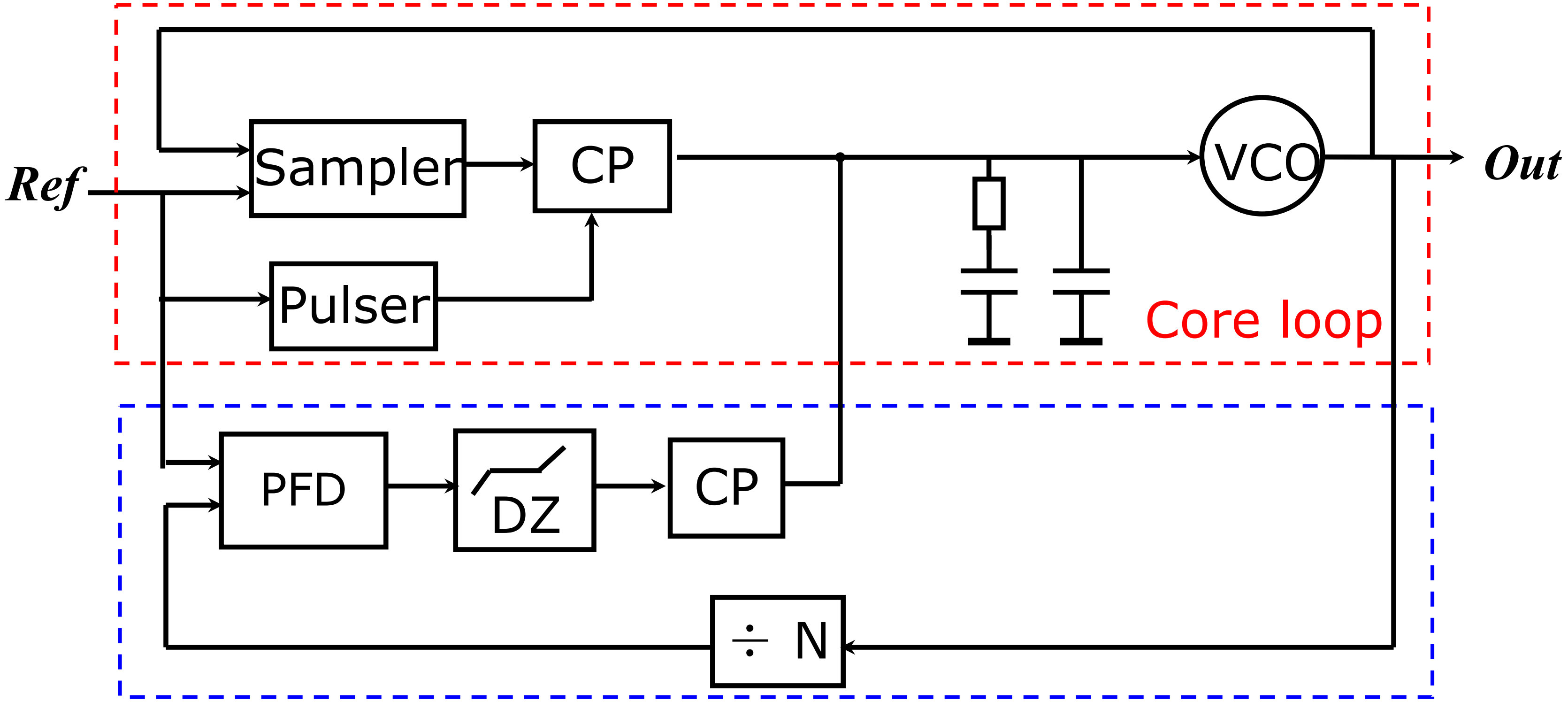
Differential Sampling





- Cancels clock feed-through & charge injection
- VCO crossing (most linear point) is locking point

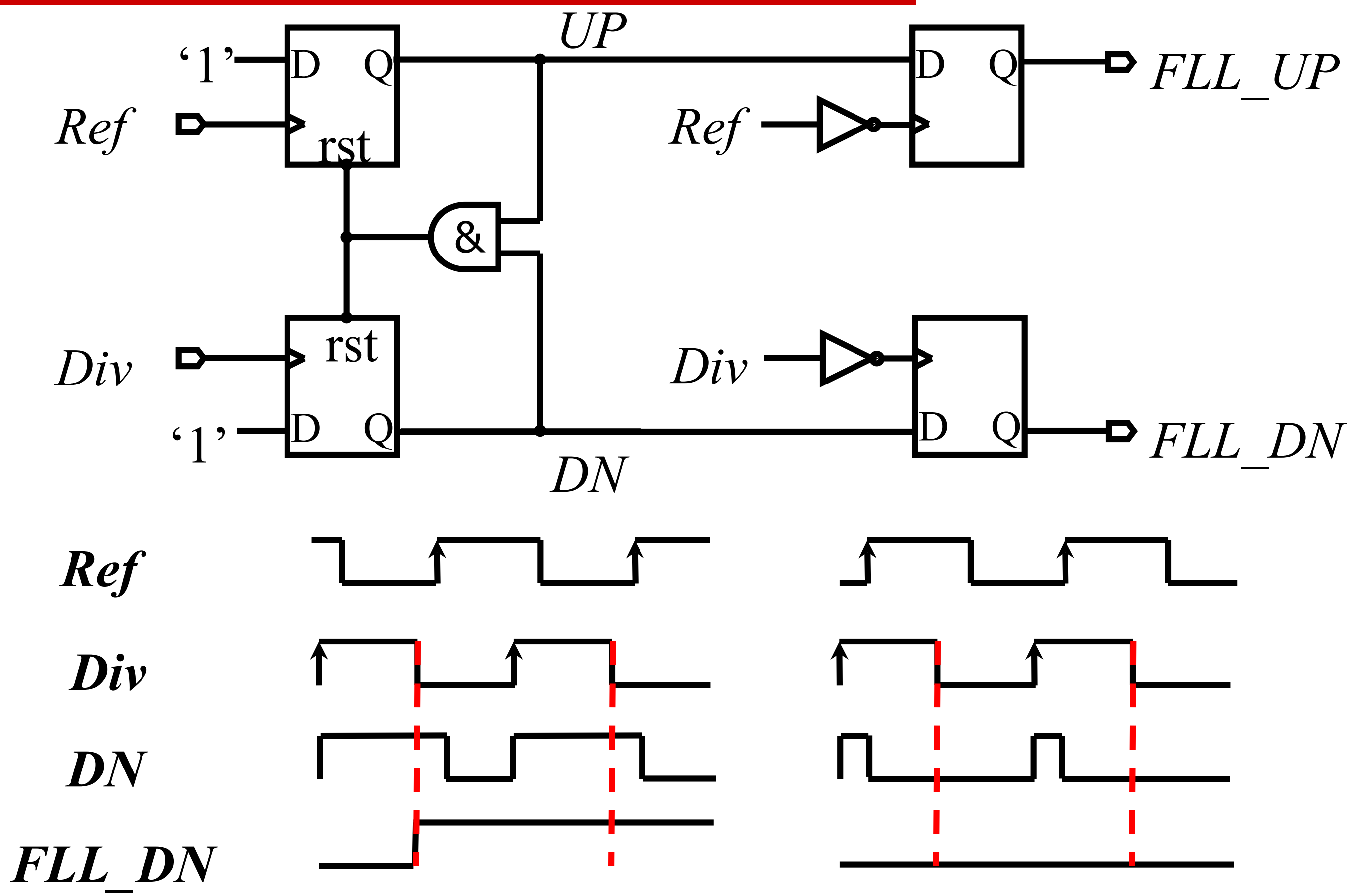
SSPLL With Frequency Locking Loop



Classical PLL with Dead Zone (DZ) as FLL

- During locking, ΔΦ > DZ, FLL has large gain, brings loop to lock
- Close to locking, ΔΦ < DZ, FLL has zero gain, not injecting noise
- FLL can also be disabled after locking to save power

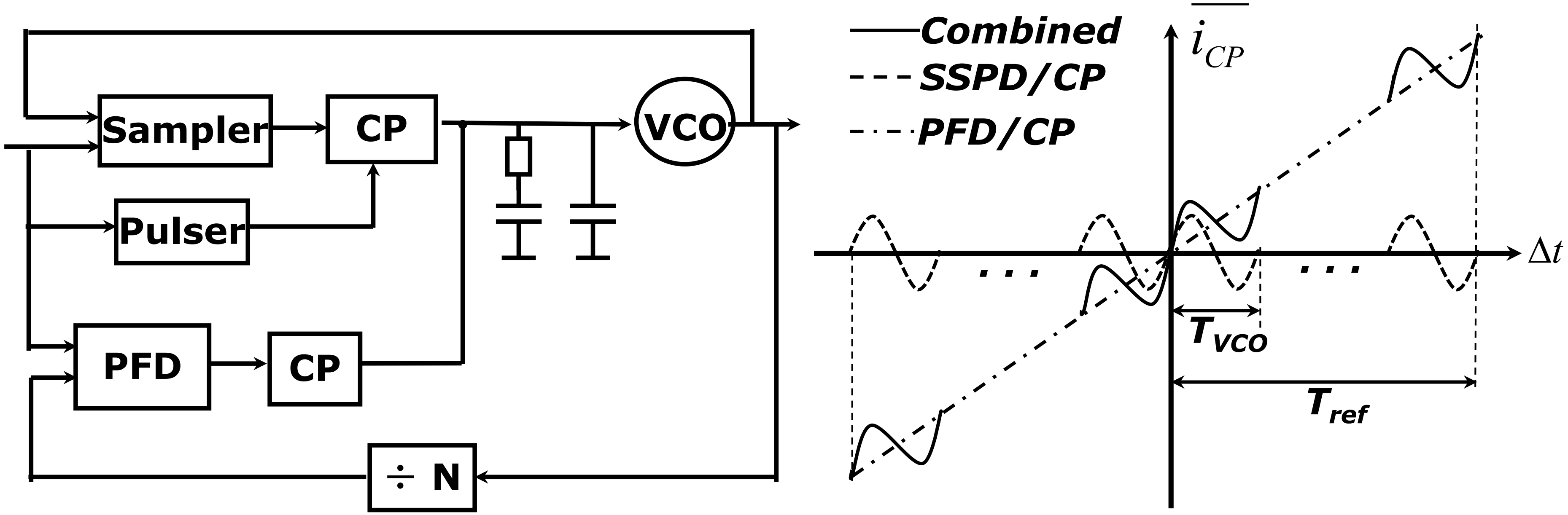
Dead Zone Creator Example



- Large phase error
- Small phase error

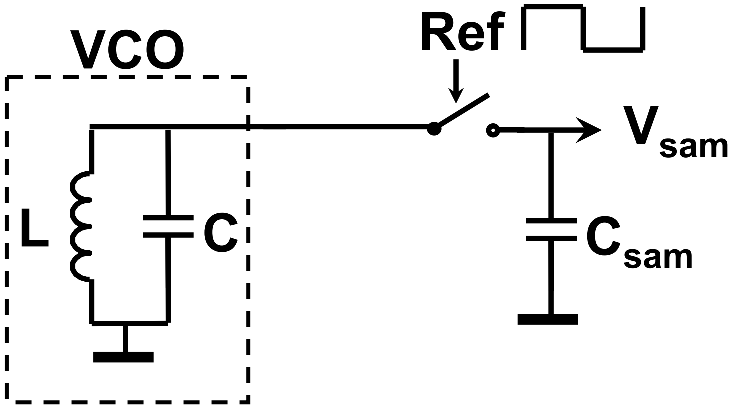
- With 50% *Ref* and *Div* duty ratio, Dead Zone is (-π, +π)

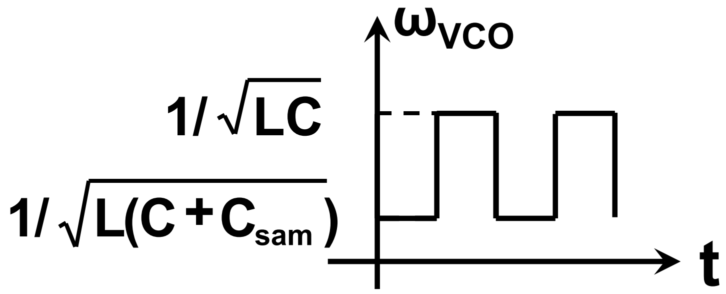
It Also Works Without Dead Zone



- FLL keeps running, more robust against disturbances [5]
- Overall characteristic is SSPD/CP and PFD/CP combined
- FLL PFD/CP injects noise but is attenuated by $(\beta_{CP,SSPD}+\beta_{CP,PFD})^2$

How To Design The SSPD





BFSK effect

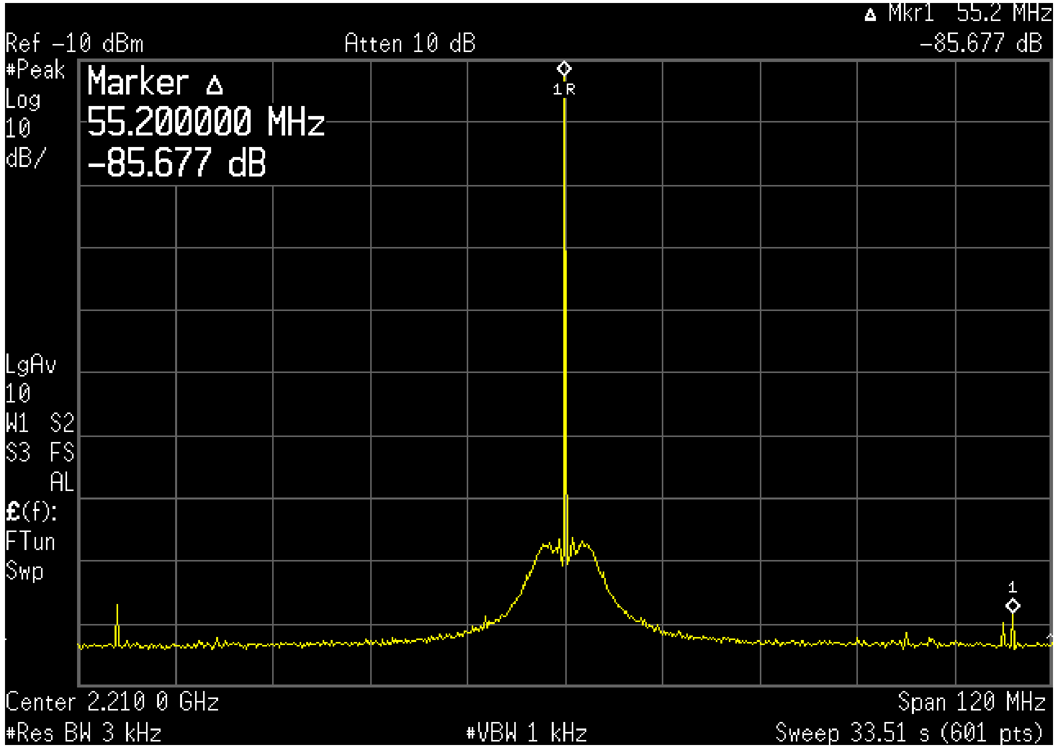
- SSPD can be designed as simple switch and cap. However, sampling activity disturbs the VCO in a few ways and need to be taken care of.
- The most noticeable disturbance to VCO is load modulation or BFSK, which would lead to large reference spurs:

$$Spur(dBc) = 20\log[\sin(\pi \cdot DR_{ref}) \cdot \frac{N}{2\pi} \cdot \frac{C_{sam}}{C}]$$

Reference Spur

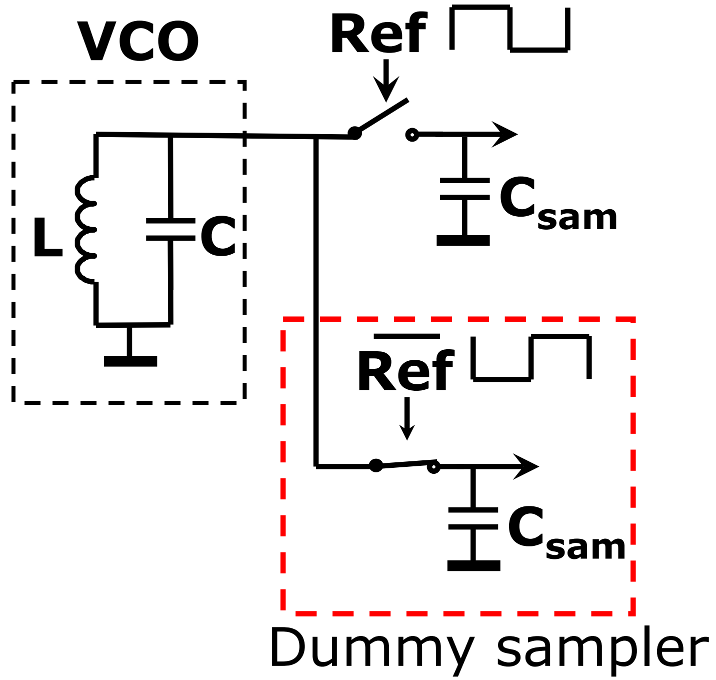
- Spurs are unwanted spurious component and would lead to deterministic jitter (versus random jitter by phase noise)

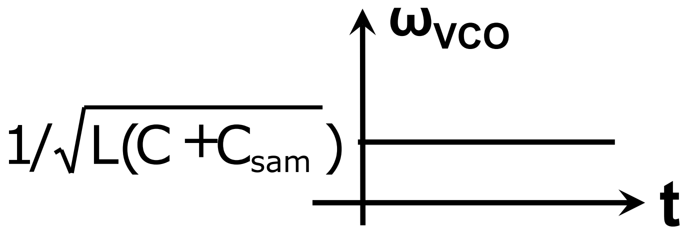
$$\Delta t_{p-p} = \frac{2}{\pi f_{out}} \times 10^{Spur(dBc)/20}$$



- A spur of -62dBc at 5GHz translates to 100fs peak-to-peak jitter

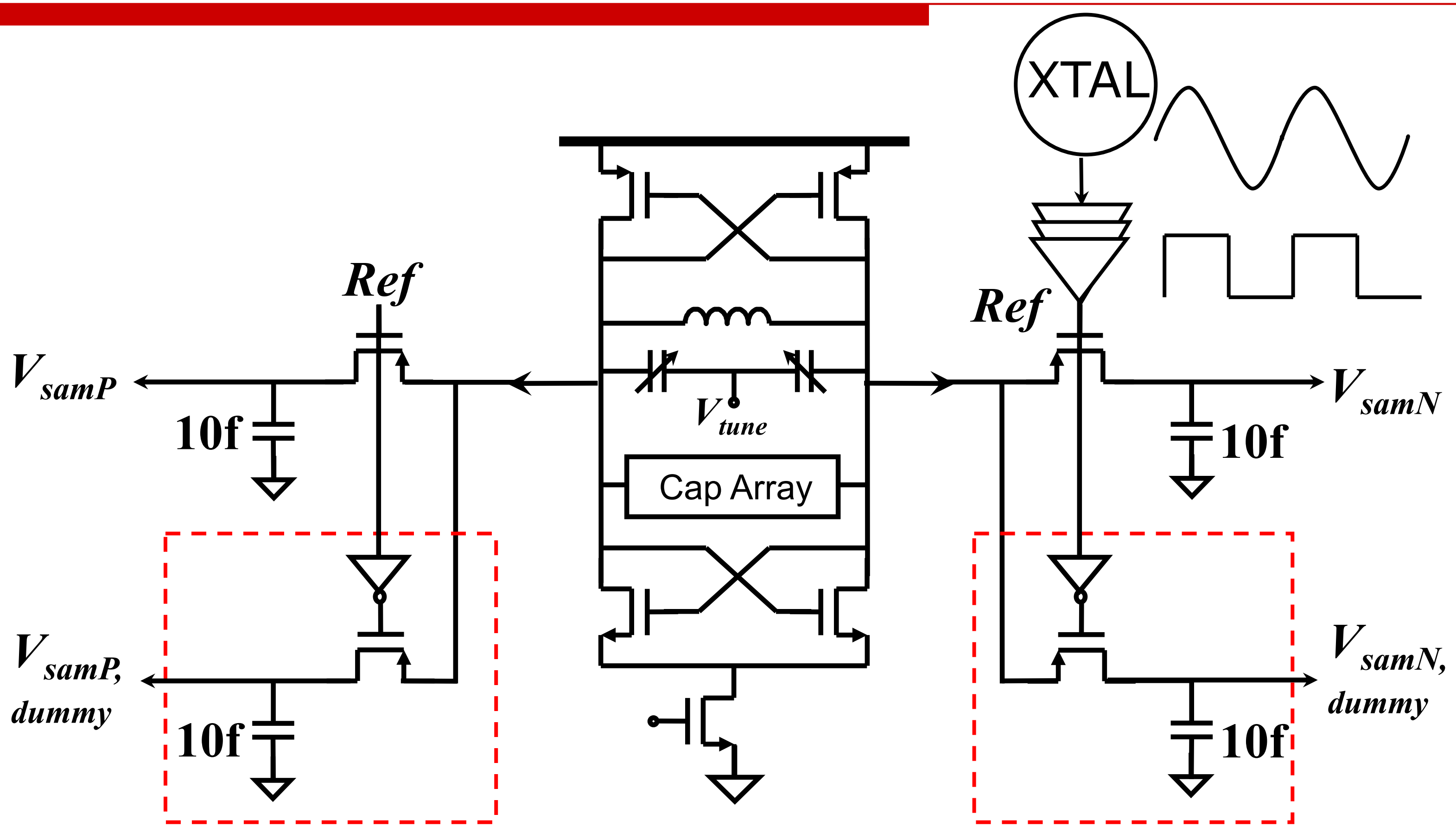
SSPD With Dummy Sampler





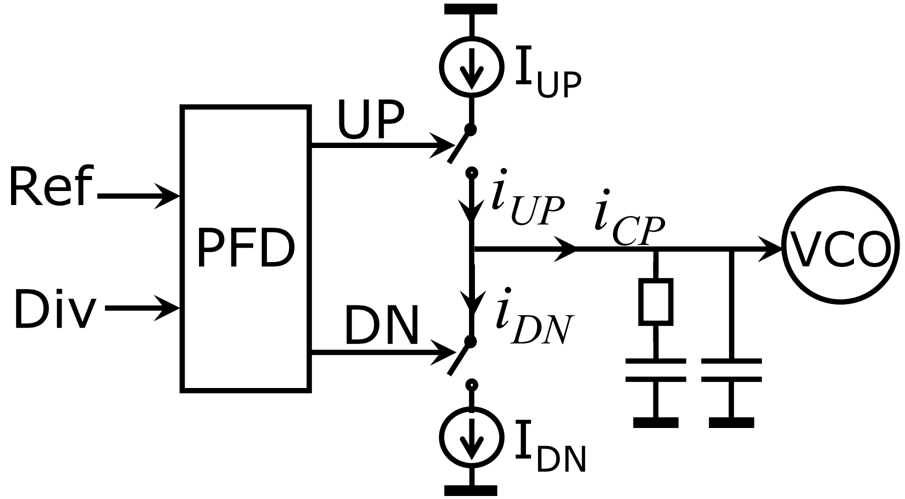
- Complementary switched dummy sampler can balance the load, and also compensate switch charge injection
- VCO-sampler buffers can be added to further reduce the spur, at the expense of power consumption

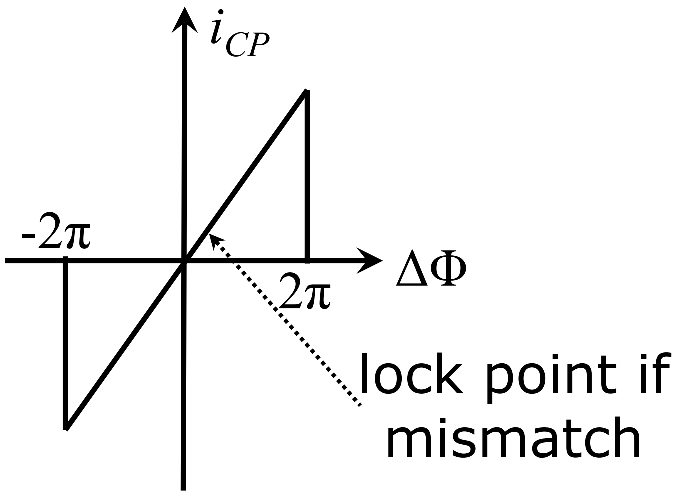
Direct VCO Sampling Design Example



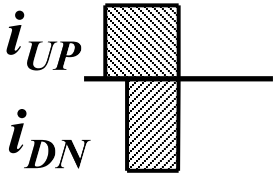
- It's possible to do direct VCO sampling to save buffer power when spur requirement is modest (e.g. -60dBc at 2.2GHz has been demonstrated in [6])

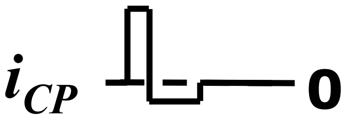
CP Design: Classical PLL



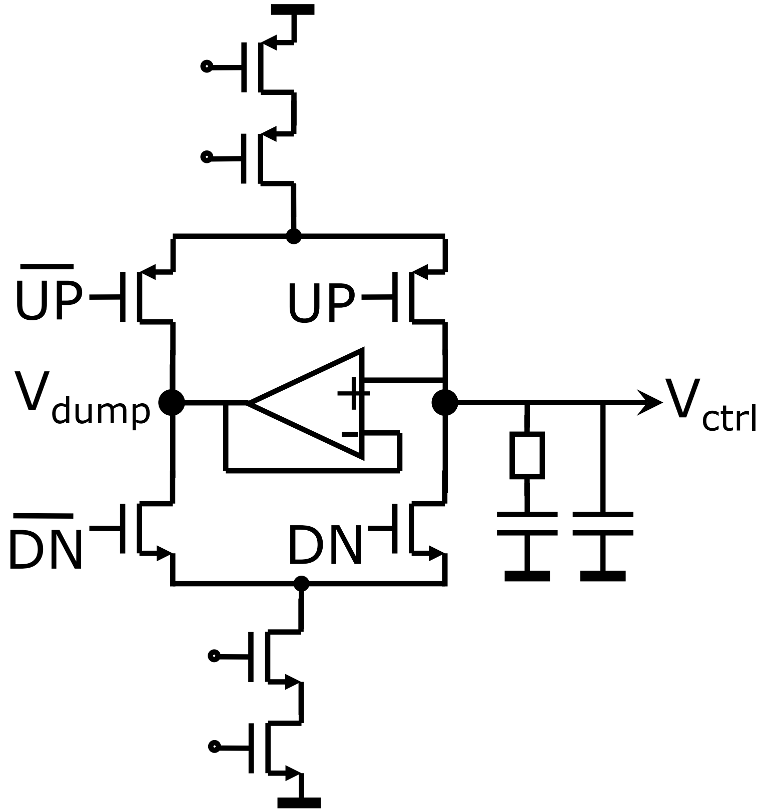


- In classical CP design, UP/DN current source has constant amplitude, but variable on-time. UP/DN mismatch has to be compensated by switch-on time difference, leading to CP output ripple and reference spur



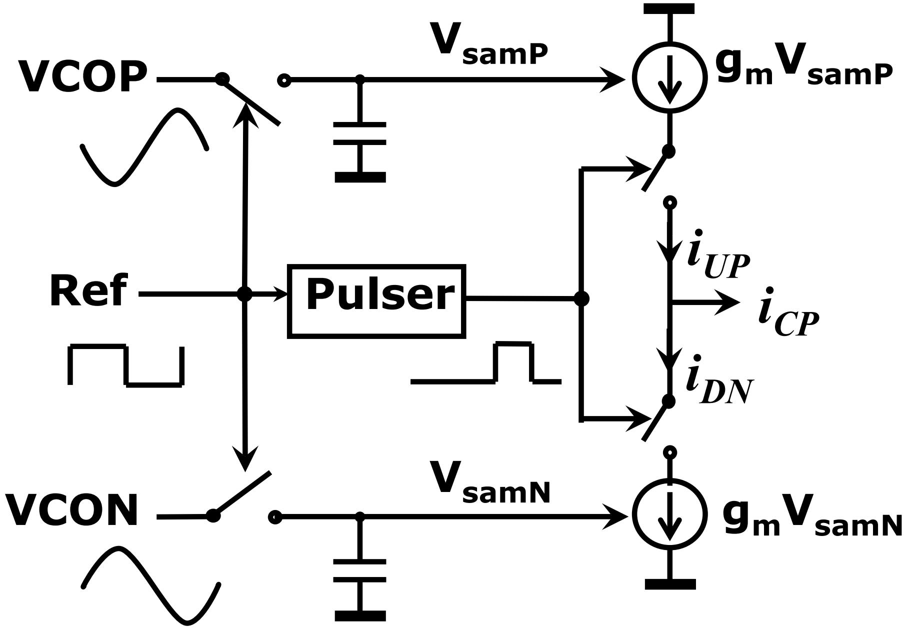


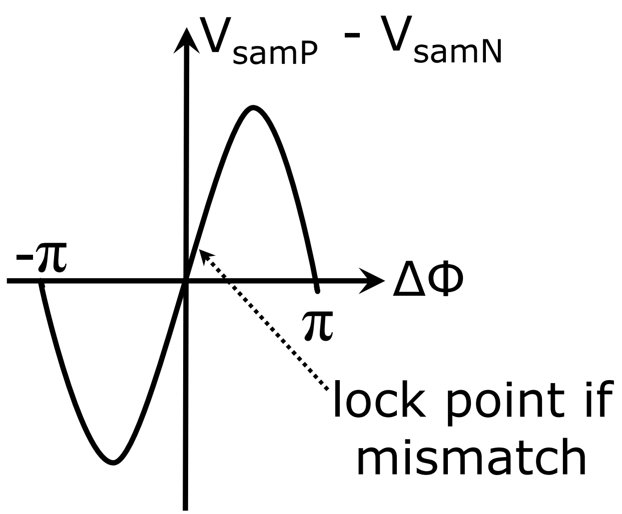
Classical Low Ripple CP Design



- Cascode transistors for high current source impedance, better matching
- Current steering, Unity Gain Buffer forces V_{dump}=V_{ctrl} to keep node voltages during switching

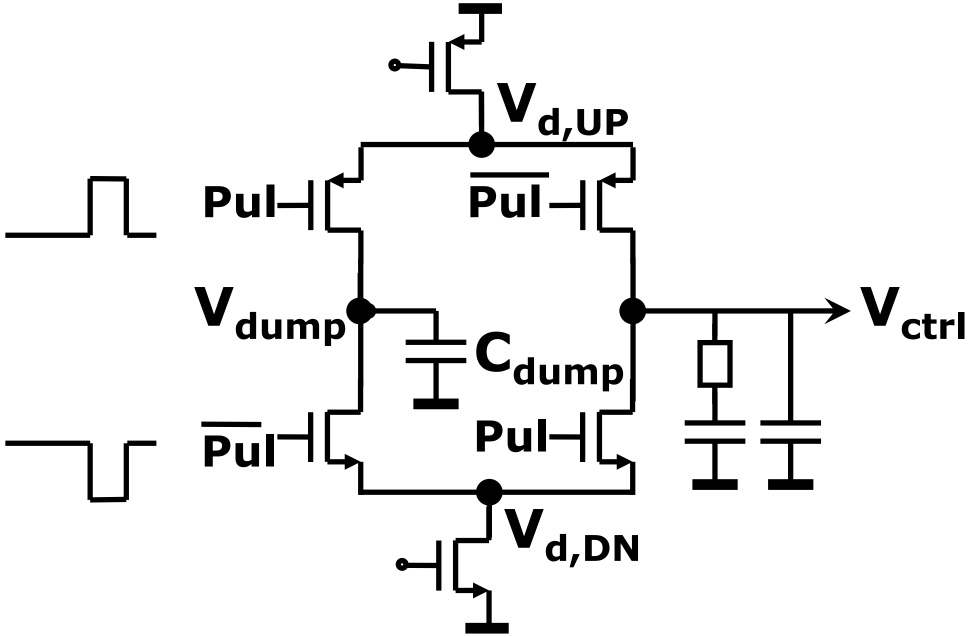
CP in SSPLL





- In SSPLL, UP/DN has constant switch-on time defined by the Pulser, but variable amplitude controlled by V_{sam}. UP/DN mismatch compensated by a shift in locking/sampling point, does not lead to CP ripple

Simple SSPLL CP Design

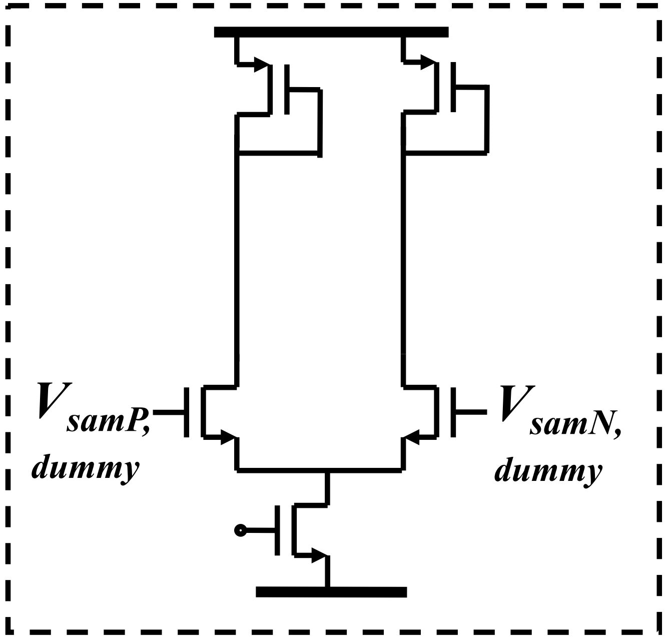


- Steer to filter: $I_{UP}=I_{DN}$ at $V_{d,UP}=V_{d,DN}=V_{ctrl}$
- Steer to C_{dump}: $I_{UP}=I_{DN}$ at $V_{d,UP}=V_{d,DN}=V_{dump}$

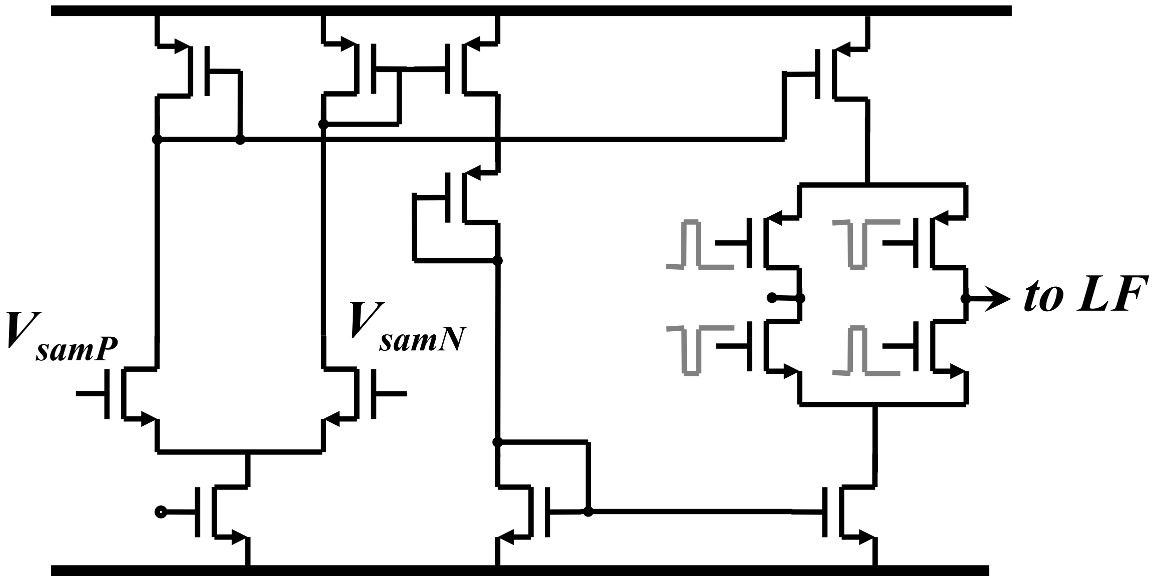
$\Longrightarrow$ Due to finite output impedance, $V_{dump}=V_{ctrl}$

- UP/DN mismatch still can't be too large to make sure locking point is close to zero crossing, but it is much more relaxed and UP/DN can be just single transistor.
- Can achieves $V_{dump}=V_{ctrl}$ without using Unity Gain Buffer

SSPLL CP Design Example



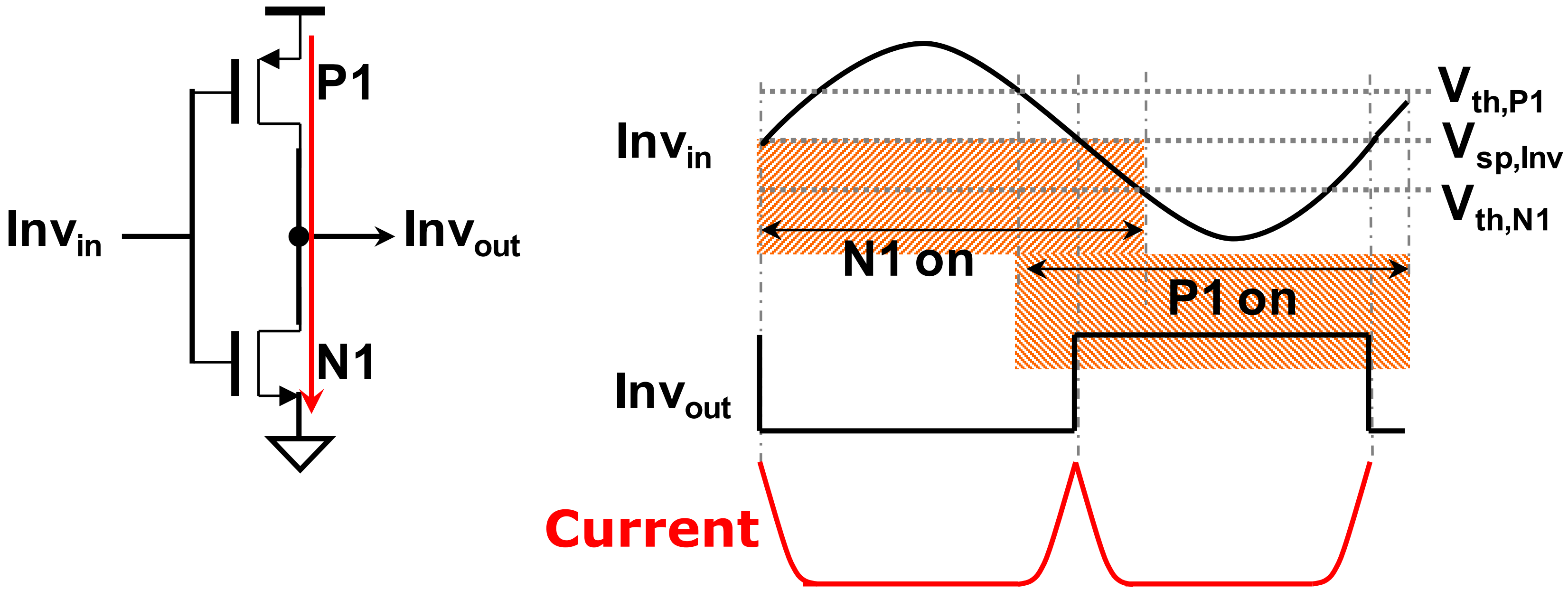
dummy CP



V → I

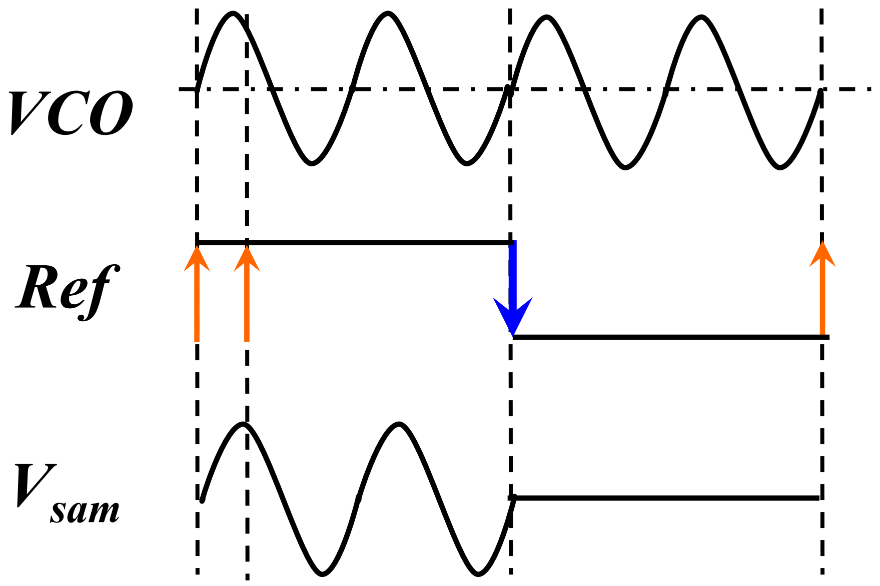
- Due to superior CP noise suppression of SSPLL, a small I_{CP} on the order of 10μA is enough to achieve very low phase noise [6]

Sampling Reference Clock Buffer



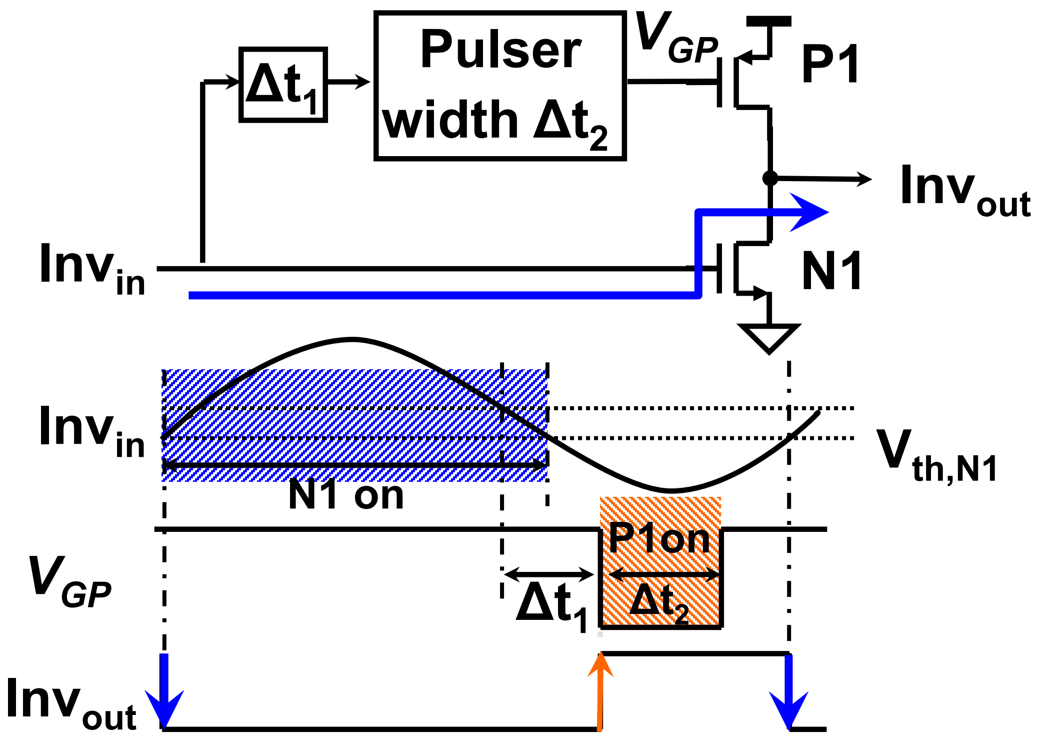
- In many applications, off-chip XTAL provides sine-wave, while PFD/SSPD needs square-wave Ref, therefore a sine-to-square buffer is needed
  - Slow sine-wave input, N1/P1 could be both on, leading to short-circuit current
  - Short-circuit current could be >90% of inverter power

How to Reduce Short-Circuit Current?



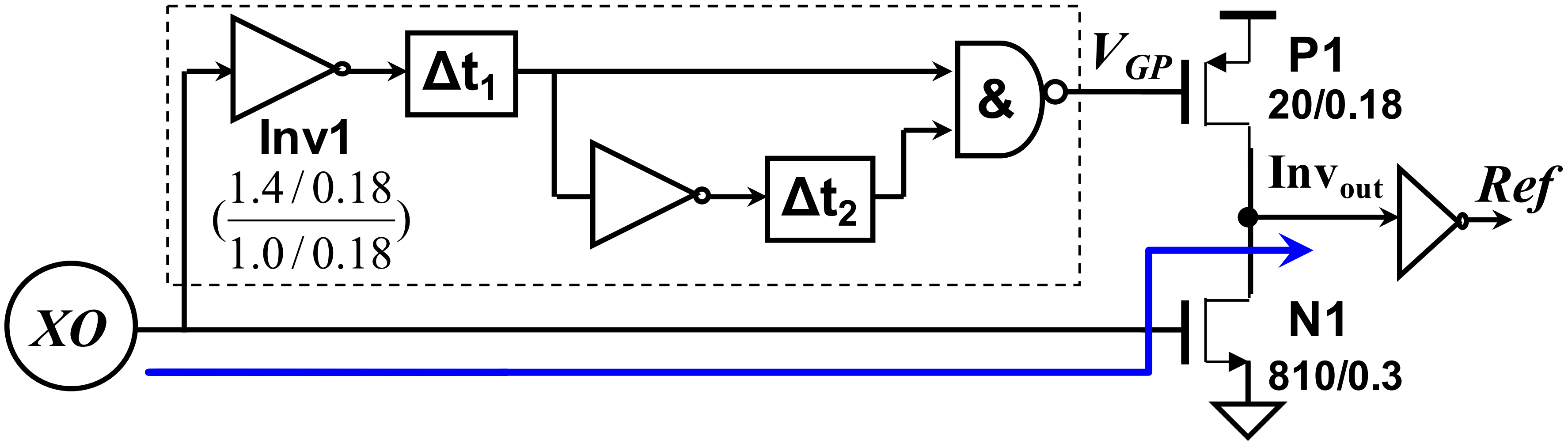
- Practical sampler: track-and-hold
  - Only the sampling edge (SE) is critical for noise
  - The tracking edge (TE) can be noisy `

Low Power Sine-to-Square Ref Buffer



- N1/P1 on-time guaranteed non-overlapping, short-circuit current eliminated
- Critical path for SE is kept clean and short

Low Power Ref Buffer Design Example [6]



- Delays are implemented with shunt-C inverters
- Transistors in critical path are sized big, others small to save power

SSPLL Generalized

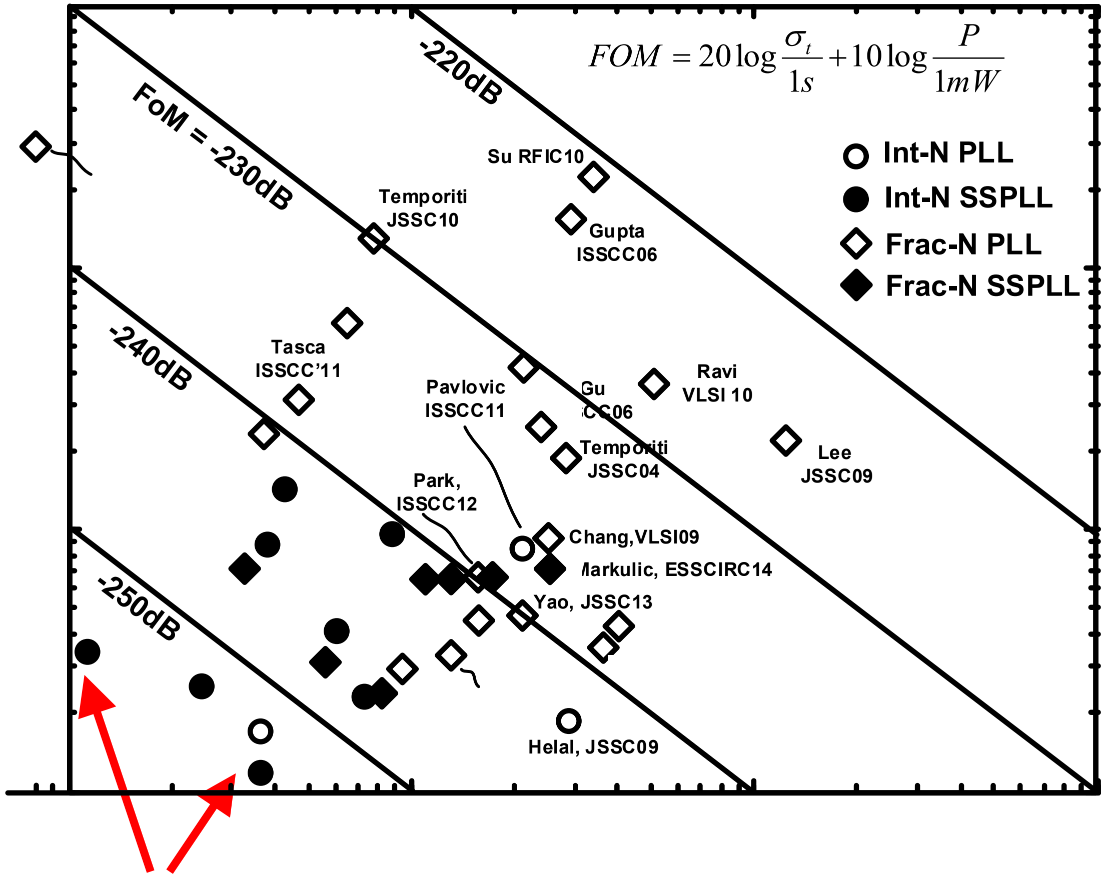
- The sampled waveform does not need to be sine-wave. The key is high detection gain by sampling high dv/dt slope .
- It works with any waveform, can also be applied to e.g. ring oscillators [7-8], but the detection gain need to be generalized:

$$\beta_{SSPD} = \frac{\Delta V_{sam}}{\Delta \phi_{VCO}} = \frac{SR_{sam}}{2\pi f_{VCO}}$$

- In more advanced process, SSPD can sample faster and utilize steeper slopes, thus benefiting from scaling. SSPLLs working at 10s-of-GHz have been demonstrated [9-10].

Low Jitter PLL Design Utopia

- All PLL need Ref clock. "PLL Utopia": only the Ref clock path contributes to non-VCO noise and power.
- In SSPLL, divider power/noise can be eliminated, CP noise is greatly suppressed, SSPD virtually consumes no power (small C_{sam}) and can even do buffer-less VCO sampling. It can thus approach this Utopia and achieve state of art performance.



Record -254dB FOM achieved at ISSCC18 using SSPLL

Outline

- PLL Basics
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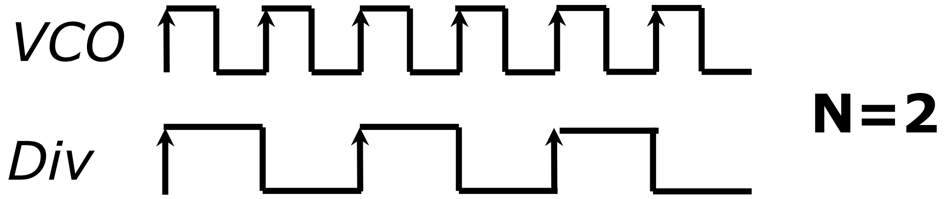
- Low Jitter Sub-Sampling PLL Architecture
- **Frac-N Sub-Sampling PLL**
- Conclusion

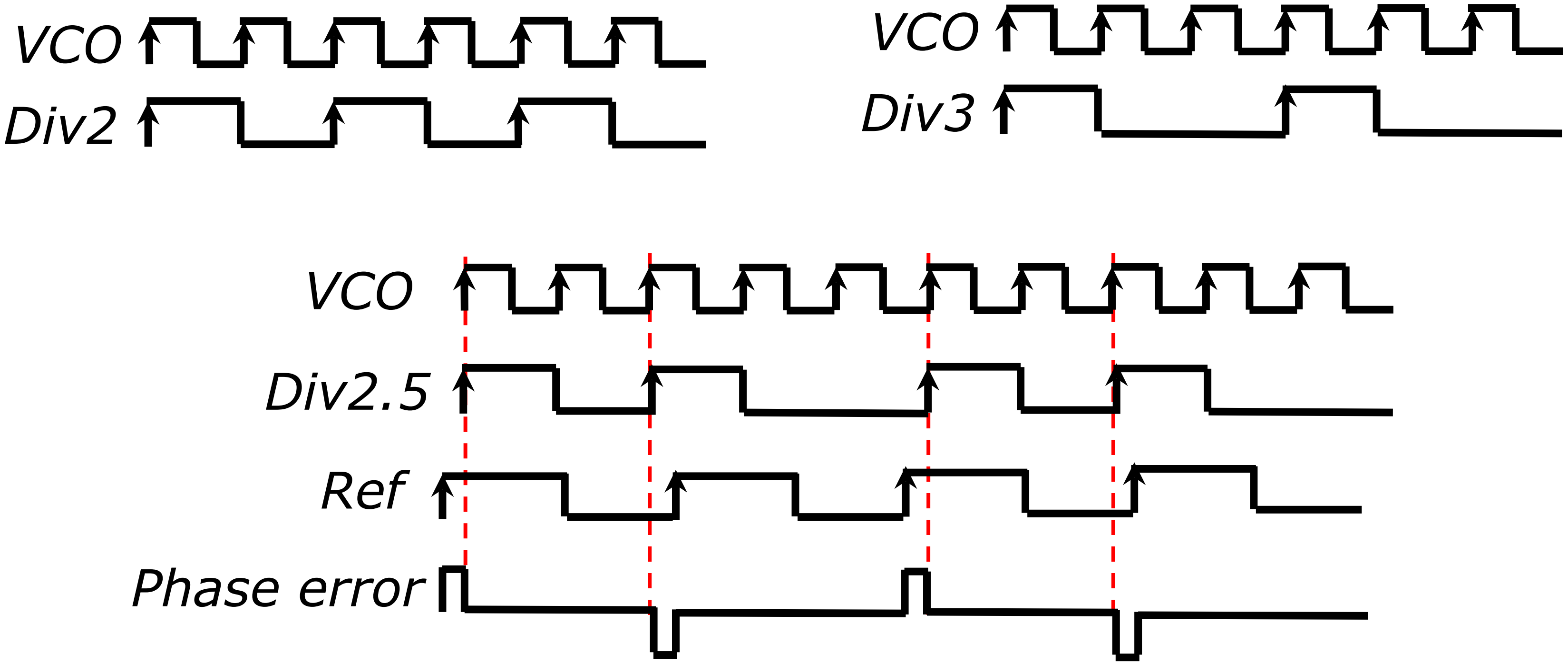
Fractional-N PLL



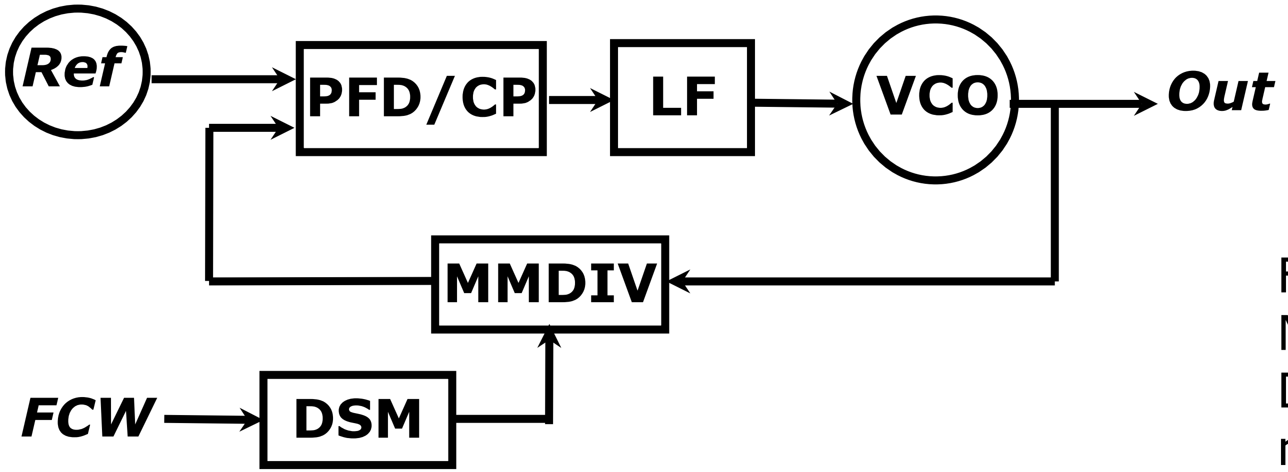
- So far we have only discussed and analyzed integer-N PLLs
- In wireless transceivers, what needed is often fractional-N PLLs: the wanted channel frequency is non integer multiple of f_{ref}
- E.g. WLAN 5825MHz channel with f_{ref}=40MHz: N=145.625

How To Realize Frac-N Division

- Frac-N division can be realized by dithering between different int-N divisions and average them out through the PLL's low pass filtering



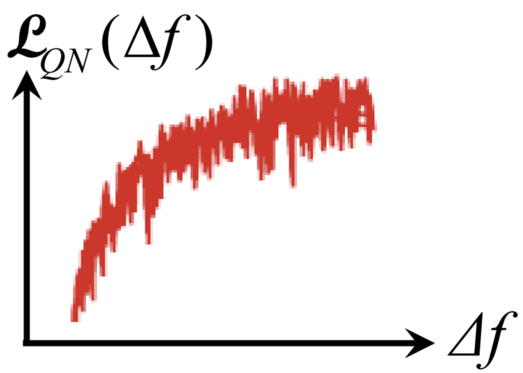
Basic Frac-N PLL Architecture



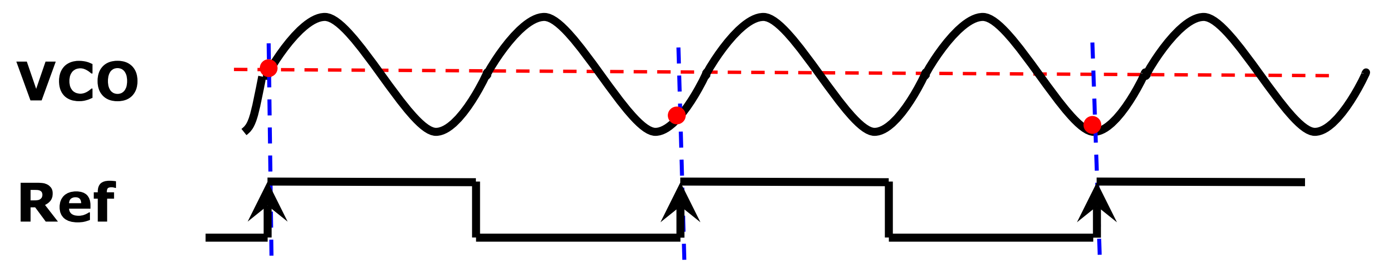
FCW: Frequency control word
MMDIV: Multi-Modulus Divider
DSM: Delta-Sigma Modulator
n: DSM order

- 2^{nd} or 3^{rd} order DSM is often used to reduce frac-N spurs
- Frac-N operation adds quantization noise

$$\mathcal{L}_{QN}(\Delta f) = \frac{(2\pi)^2}{12 f_{ref}} \{2\sin(\pi \frac{\Delta f}{f_{ref}})\}^{2(n-1)}$$

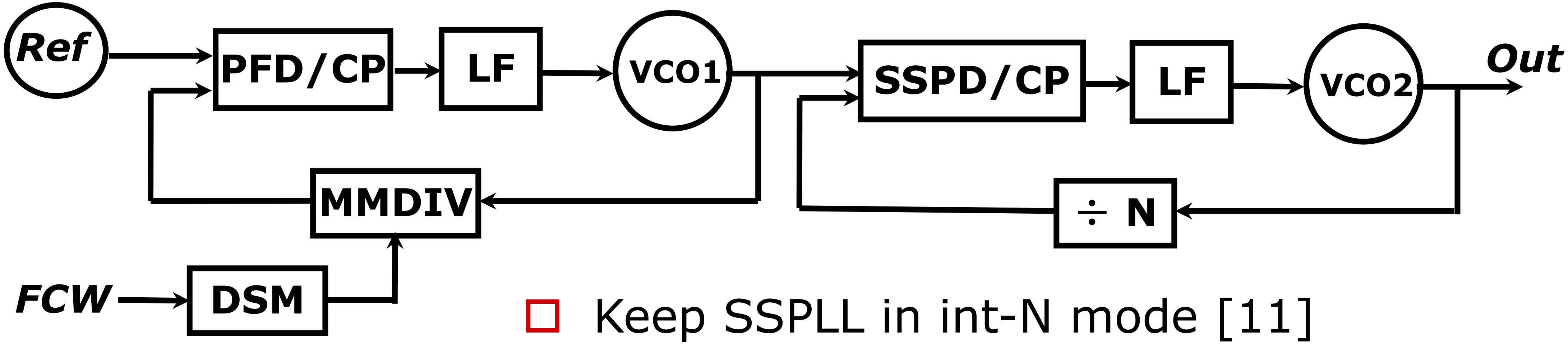


Can SSPLL Work As Frac-N ?

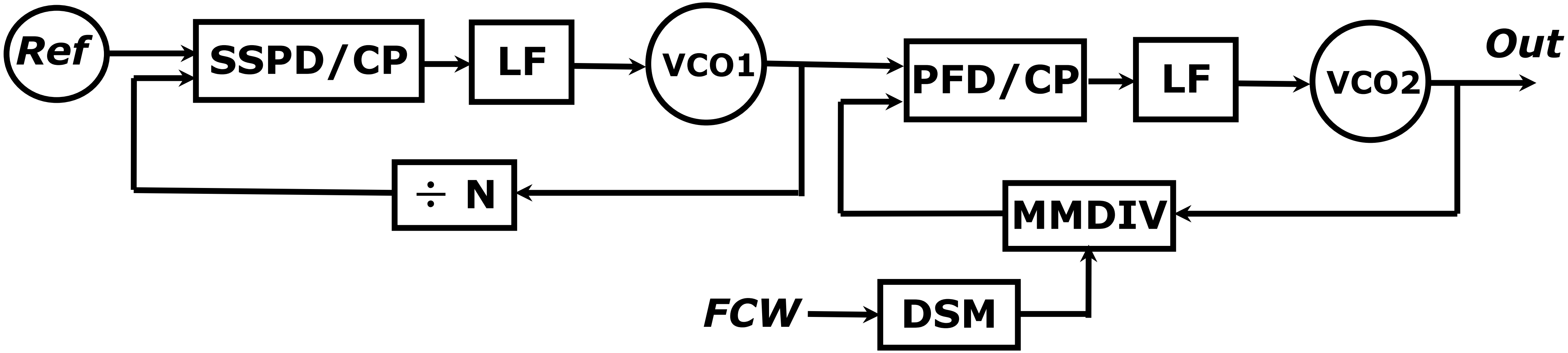


- SSPD is linear only around zero crossing, ok for int-N
- In frac-N PLL the sampling point is all over the VCO waveform even in locked state, SSPD wouldn't work properly

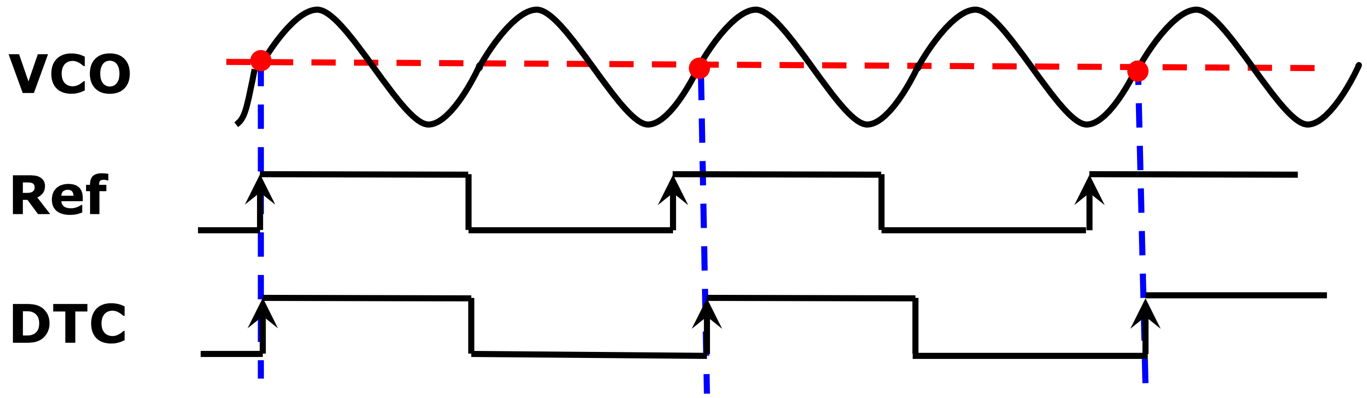
Cascade SSPLL With Frac-N PLL



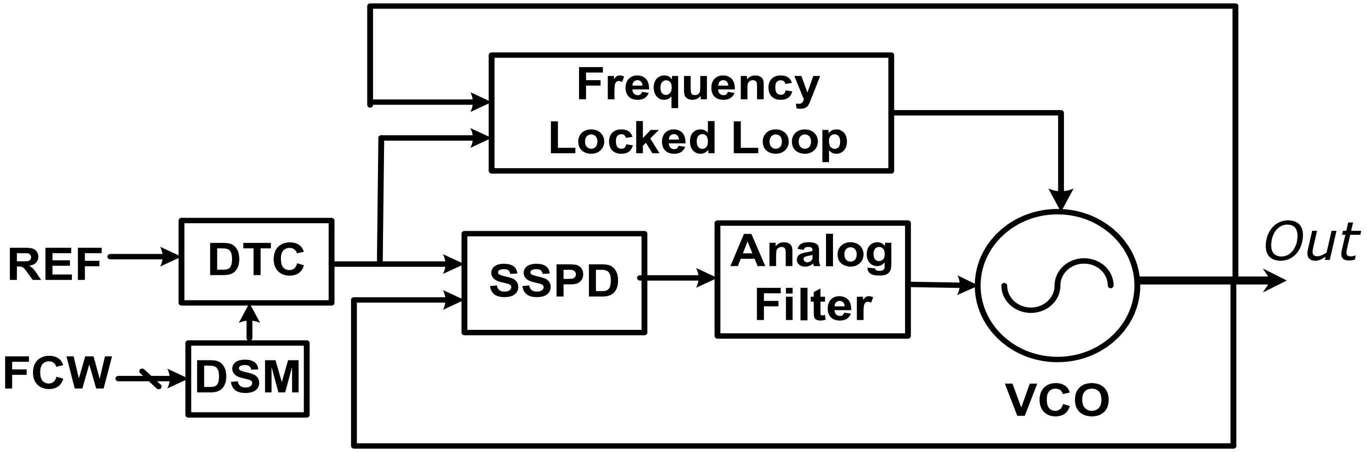
- Keep SSPLL in int-N mode [11]



Digitla-to-Time Converter Assisted Frac-N SSPLL



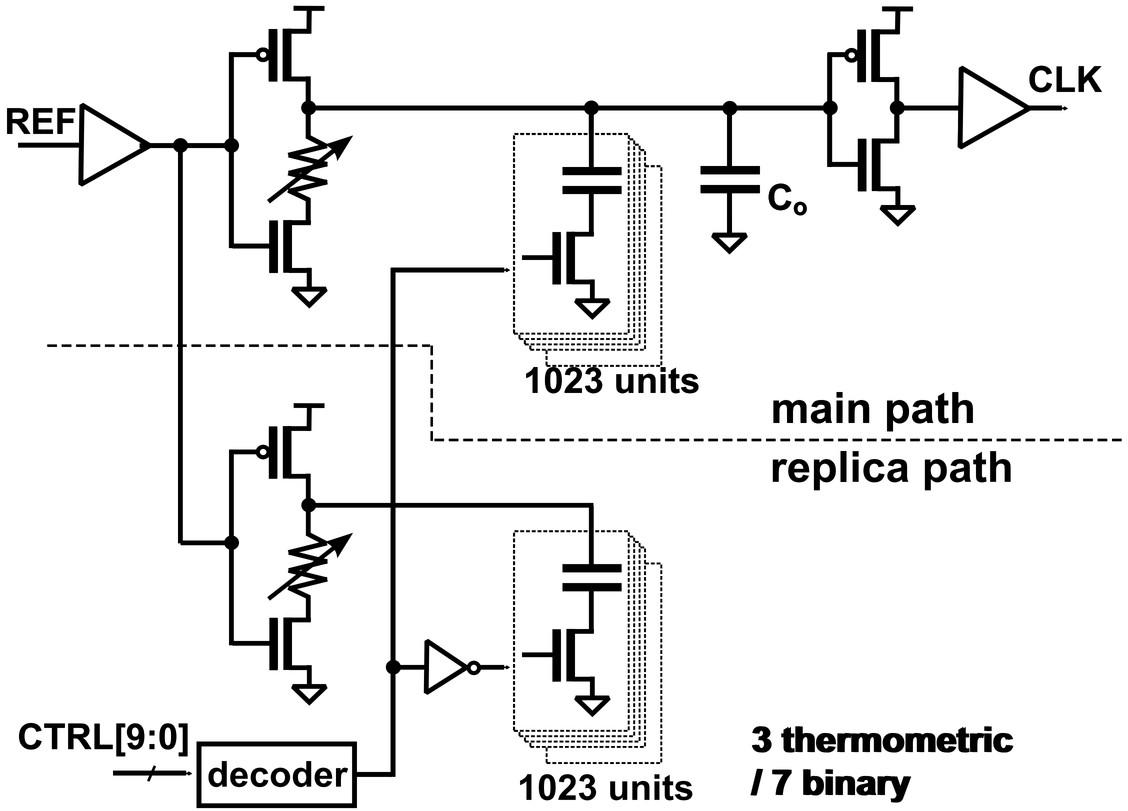
- DTC modulates Ref edge, SSPD sees small Δt, works as if it's int-N mode even though the entire system is frac-N mode



DTC also reduces QN by

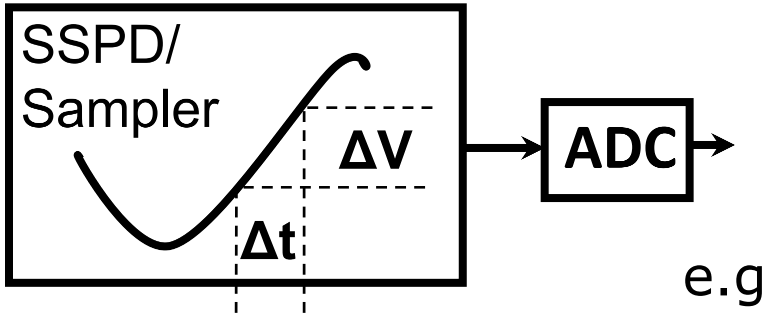
$$20\log\frac{\Delta t_{DTC}}{T_{VCO}}$$

10-bit DTC Design Example



- RC delay based DTC [12]
- Coarse tuning via R, fine tuning via cap-bank
- Replica path lower code dependent supply ripple

SS Time-to-Digital Converter and Digital SSPLL

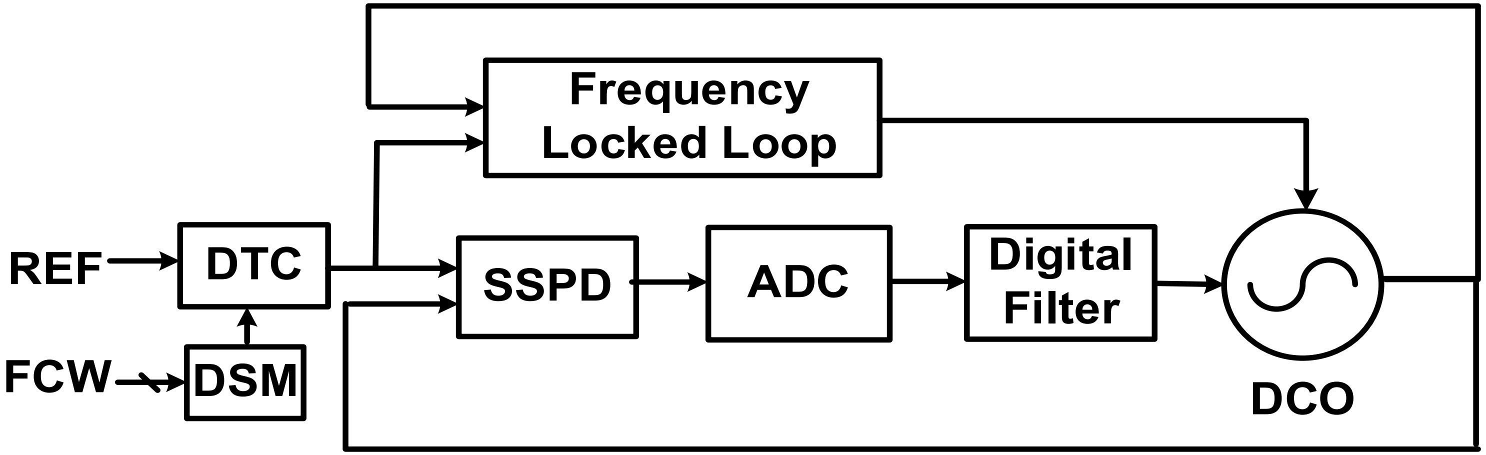


$$\Delta t_{TDC} = \frac{\Delta V_{ADC\,LSB}}{dV/dt}$$

e.g. $\Delta t_{TDC} = \frac{1mV}{10GV/s} \approx 0.1ps$

100x smaller than gate delay

- Quantize SSPD output with ADC leads to high resolution SSTDC, can be used to build a digital SSPLL [13-16]



Outline

- PLL Basics
- Classical CP PLL Analysis and Optimization
- Low Jitter Sub-Sampling PLL Architecture
- Frac-N Sub-Sampling PLL
- **Conclusion**

Summary and Conclusion

- There is fundamental tradeoff between PLL jitter and power. The performance can be benchmarked using PLL FOM.
- Optimum PLL performance needs optimization from both block level and system level (power budgeting, optimum BW)
- Sub-Sampling PLL is proven to be low jitter architecture
  - High phase detection gain, low PD/CP noise, possibly no divider noise
  - Can operate in Frac-N mode
  - Can be digitized utilizing high resolution sub-sampling TDC

Papers to See This Year

Session 15 "RF PLLs" Relevant Papers:

- 15.1: Constant-Slope DTC for Frac-N PLL
- 15.3: Sampling-TDC/ADC based digital PLL
- 15.6: Type-I Sub-Sampling PLL with -254dB FOM
- 15.7: Type-I Reference Sampling PLL with -253.5dB FOM

Session 23 "LO Generation" Relevant Paper:

- 23.1: Frac-N PLL for 5G communication
- 23.5, 23.6: VCO design
- 23.7: Classical CP PLL with 54fs rms jitter in 16nm Finfet

Suggested References

1. P. Kinget, “Integrated GHz voltage controlled oscillators,” *Analog Circuit Design: (X)DSL and Other Communication Systems; RF MOST Models; Integrated Filters and Oscillators*, W. Sansen, *et al.*, Ed. Boston, MA: Kluwer, 1999, pp. 353-381.
2. A. A. Abidi, “Phase noise and jitter in CMOS ring oscillators,” IEEE J.Solid-State Circuits, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.
3. X. Gao, E. Klumperink, P. J. F. Geraedts and B. Nauta, “Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops,” *IEEE Trans. Circuits Syst. II*, vol. 56, no.2, pp. 117-121, Feb. 2009.
4. X. Gao, E. Klumperink, M. Bohsali and B. Nauta, “A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is not Multiplied by N^2,” *IEEE J. Solid-State Circuits,* vol. 44, no.12, pp. 3253-3263, Dec. 2009.
5. C.-W. Hsu, K. Tripurari, S.-A. Yu and P. R. Kinget, “A Sub-Sampling-Assisted Phase-Frequency Detector for Low-Noise PLLs With Robust Operation Under Supply Interference,” *IEEE Trans. Circuits Syst. I,* vol.62, no.1, pp.90-99, Jan. 2015.
6. X. Gao, E. Klumperink, G. Socci, M. Bohsali and B. Nauta, “A 2.2GHz Sub-Sampling PLL with 0.16ps_{rms} Jitter and -125dBc/Hz In-band Phase Noise at 700μW Loop-Components Power,” *IEEE Symposium on VLSI Circuits*, pp. 139-140, Jun. 2010.
7. S. D. Vamvakos, *et. al.*, “A 8.125–15.625 Gb/s SerDes using a sub-sampling ring-oscillator phase-locked loop," *IEEE Custom Integrated Circuits Conference (CICC)*, paper 10.1, Sept. 2014.
8. K. Sogo, A. Toya and T. Kikkawa, “A ring-VCO-based sub-sampling PLL CMOS circuit with −119 dBc/Hz phase noise and 0.73 ps jitter," *IEEE European Solid State Circuits Conference (ESSCIRC),* pp.253-256, Sept. 2012.
9. X. Yi, C. C. Boon, J. Sun, N. Huang and W. M. Lim, “A low phase noise 24/77 GHz dual-band sub-sampling PLL for automotive radar applications in 65 nm CMOS technology,” *IEEE Asian Solid-State Circuits Conference (A-SSCC),* pp.417-420, Nov. 2013.
10. T. Siriburanon, *et. al.*, “A 60-GHz sub-sampling frequency synthesizer using sub-harmonic injection-locked quadrature oscillators,” *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp.105-108, Jun. 2014.

Suggested References Cont’d

11.W. EI-Halwagy, A. Nag, P. Hisayasu, F. Aryanfar, P. Mousavi, M. Hossain, "A 28GHz quadrature fractional-N synthesizer for 5G mobile communication with less than 100fs jitter in 65nm CMOS", IEEE Radio Frequency Integrated circuits Symposium (RFIC), pp. 118-121, 2016.
12.N. Markulic, K. Raczkowski, P. Wambacq and J. Craninckx, “A 10-bit, 550-fs step Digital-to-Time Converter in 28nm CMOS,” IEEE European Solid State Circuits Conference (ESSCIRC), pp.79-82, Sept. 2014.
13.T. Siriburanon, *et. al.*, “A 2.2GHz −242dB-FOM 4.2mW ADC-PLL using digital sub-sampling architecture," *IEEE Solid-State Circuits Conference - (ISSCC)*, paper 25.2, Feb. 2015.
14.Z. Ru, P. Geraedts, E. Klumperink and B. Nauta, “A 12GHz 210fs 6mW Digital PLL with Sub-sampling Binary Phase Detector and Voltage-Time Modulated DCO,” IEEE Symp. VLSI Circuits, pp. 194-195, June 2013.
15.Z.-Z. Chen, *et. al.*, “Sub-sampling all-digital fractional-N frequency synthesizer with −111dBc/Hz in-band phase noise and an FOM of −242dB,” *IEEE Solid- State Circuits Conference - (ISSCC)*, paper 14.9, Feb. 2015.
16.W.-S. Chang, P,-C, Huang and T.-C. Lee, “A Fractional-N Divider-Less Phase-Locked Loop With a Subsampling Phase Detector,” IEEE J. Solid-State Circuits, vol.49, no.12, pp.2964-2975, Dec. 2014.
17. X. Gao, E. Klumperink, G. Socci, M. Bohsali and B. Nauta, “Spur Reduction Techniques for Phase-Locked Loops Exploiting a Sub-Sampling Phase Detector,” *IEEE J. Solid-State Circuits,* vol. 45, no.9, pp. 1809-1821, Sept. 2010.
18.A. T. Narayanan, et. al., “A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator with a FoM of -246dB”, IEEE European Solid State Circuits Conference (ESSCIRC), pp.380-383, Sept. 2015.
19. X. Gao, “Low Jitter Low Power Phase Locked Loops Using Sub-Sampling,” PhD thesis, University of Twente, ISBN-978-90-365-3022-4, 2010.
20.J. A. Crawford, Frequency Synthesizer Design Handbook. Boston, MA: Artech House, 1994.
21.C. S. Vaucher, Architectures for RF Frequency Synthesizers. Boston, MA: Kluwer, 2002.