Clocking, clock distribution, and clock management in wireline and wireless subsystems

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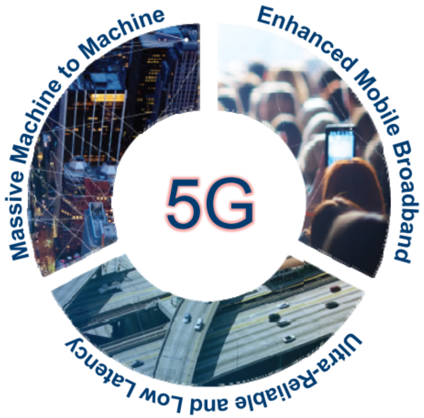
Self Introduction

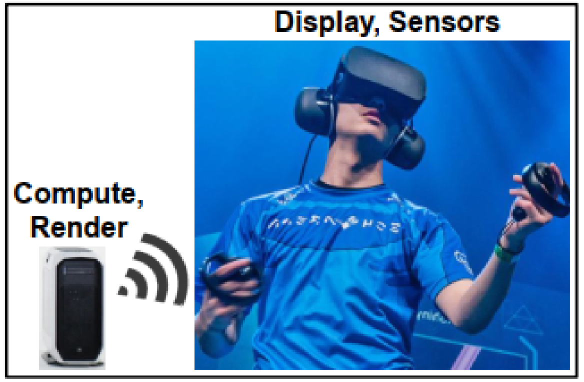
- B.S. and M.S. degrees from Sharif University of Technology, Iran, in 1995 and 1997
- Ph.D. degree from University of California, Los Angeles, in 2003
- "Kavoshgaran Consulting Engineers", Tehran, Iran (1997-1999)
- Intel corporation, Hillsboro, OR (2003-present)
- My interests are in clock synthesis/recovery circuits (PLLs and DLLs), variation-tolerant circuits, optical/electrical and memory I/O links

Bandwidth Growth

	More Internet Users	More Devices & Connections	Faster Broadband Speeds	More Video Viewing
2017	3.4 Billion	18.0 Billion	39.0 Mbps	75% of Traffic
2022	4.8 Billion	28.5 Billion	75.4 Mbps	82% of Traffic

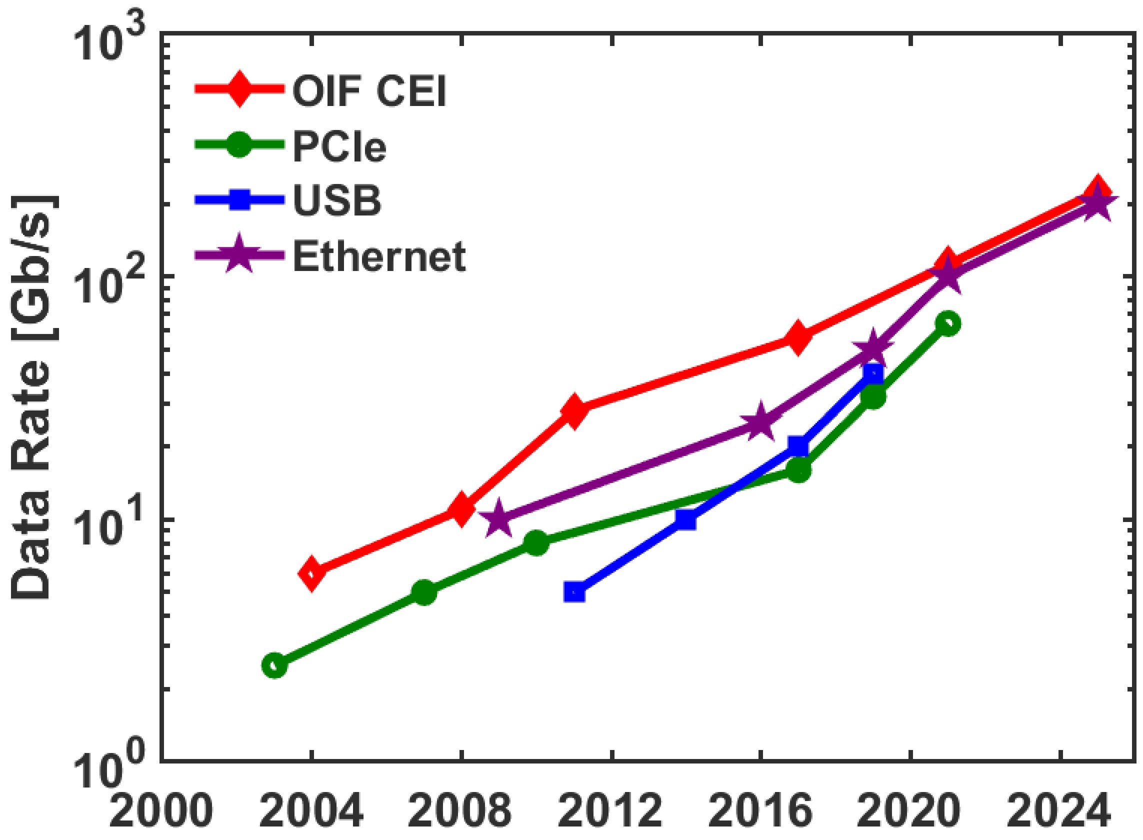
- ☐ Many users, many devices and connections
- ☐ Bandwidth demand is growing rapidly
  - ■ Worldwide international bandwidth, between 2017 and 2019, is more than doubled to reach ~1,500 Tbps*.





* Source: TeleGeography; This data does not reflect the impact of COVID-19.

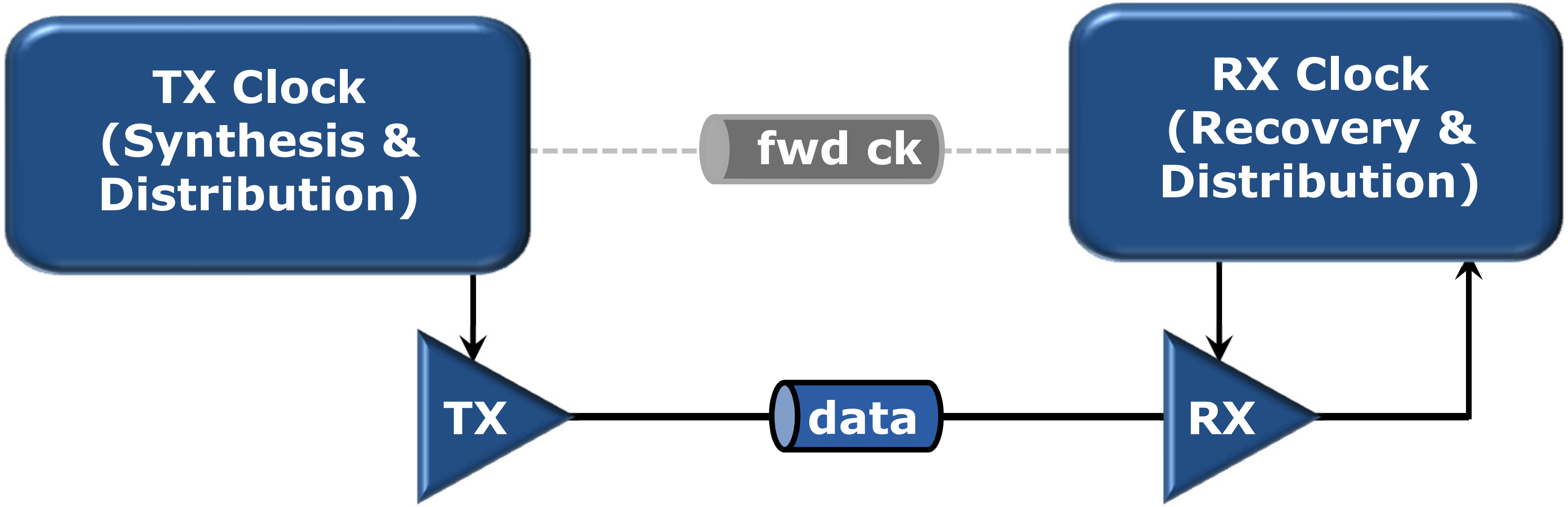
Wireline Per Lane Data Rate Trends



T. Musah, "Wireline Link Standard," [Online]. Available: https://mics.engineering.osu.edu/iostandards

- Aggressive data rate scaling
  - Per-lane data rate doubles every 3 years across diverse I/O standards

Multi-Gb/s Wireline Connectivity



- To enable multi-Gb/s
  - Improved channel and co-optimized TX & RX equalization
  - TX clock synthesis to retime data at the TX
  - Clock and data recovery to sample data at the receiver
  - Optimized TX and RX clock jitter

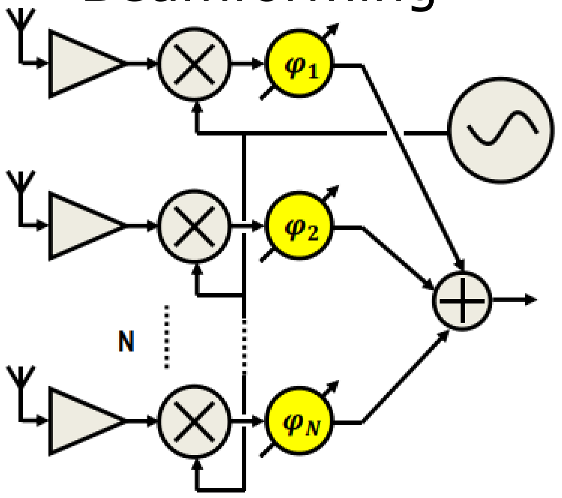
Clocking Design in Microprocessor Systems

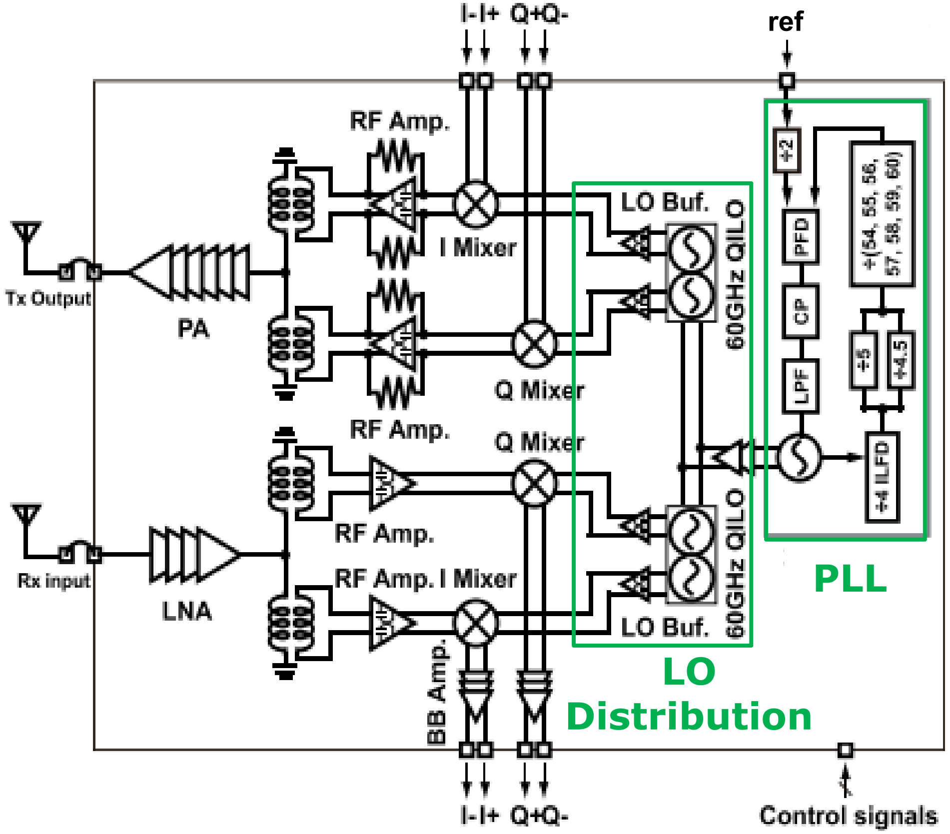
- Process technology optimized for low-power digital design
  - Suboptimum transistors (Rout, gain, ft, matching)
  - Feature limited (inductors, resistors, and capacitors)
- Process scaling
  - Variation
  - Density, reliability and power constraints
- Platform
  - Bandwidth limited channel
  - Supply/substrate noise
  - Low-cost low-quality reference clock

Challenges in generating and distributing high-quality clock

Multi-Gb/s Wireless Connectivity

Beamforming

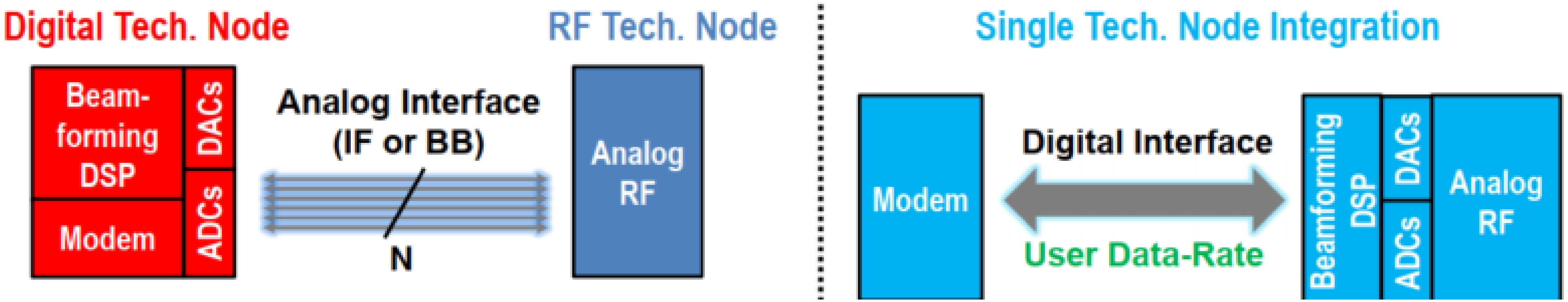




- To enable multi-Gb/s
  - mmWave phased arrays (beamforming)
  - Channel-bonding capability and higher order modulation
  - Optimized phase noise of local oscillator (LO) and distribution
  - Clock jitter of analog-to-digital converter (ADC)/digital-to-analog converter (DAC)

Clocking Design in Wireless Systems

S. Pellerano, et al. "A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver …", ISSCC 2019



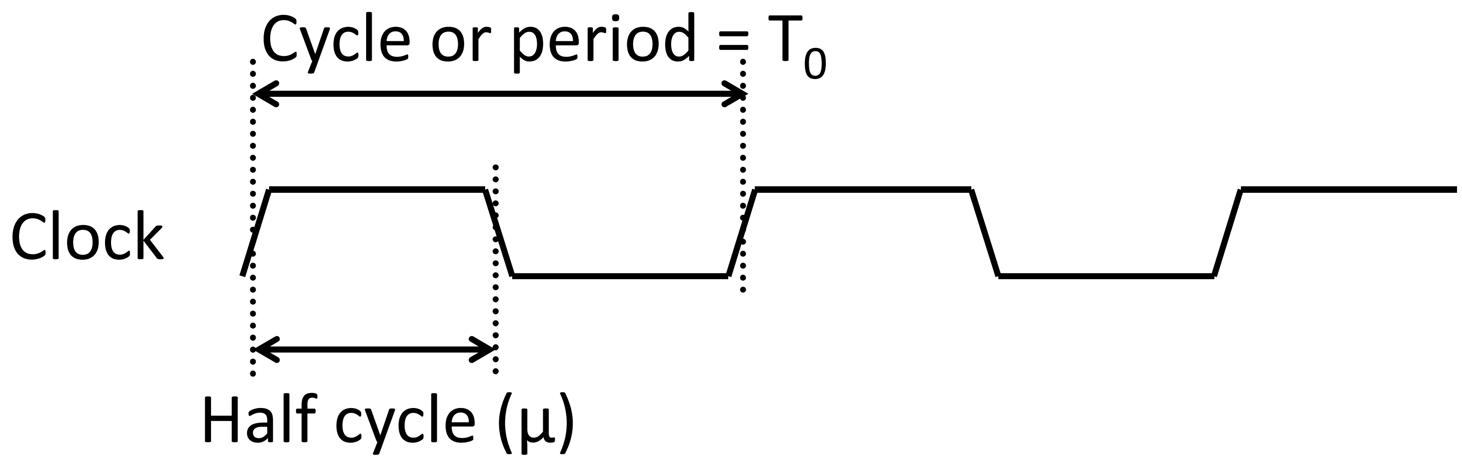
- Process technology requirement: RF performance vs. scalability (IO & DSP)
- Process scaling
  - Variation, density, reliability and power constraints
- Platform
  - LO leakage, supply/substrate noise

Design tradeoffs in generating and distributing high-quality LO

Outline

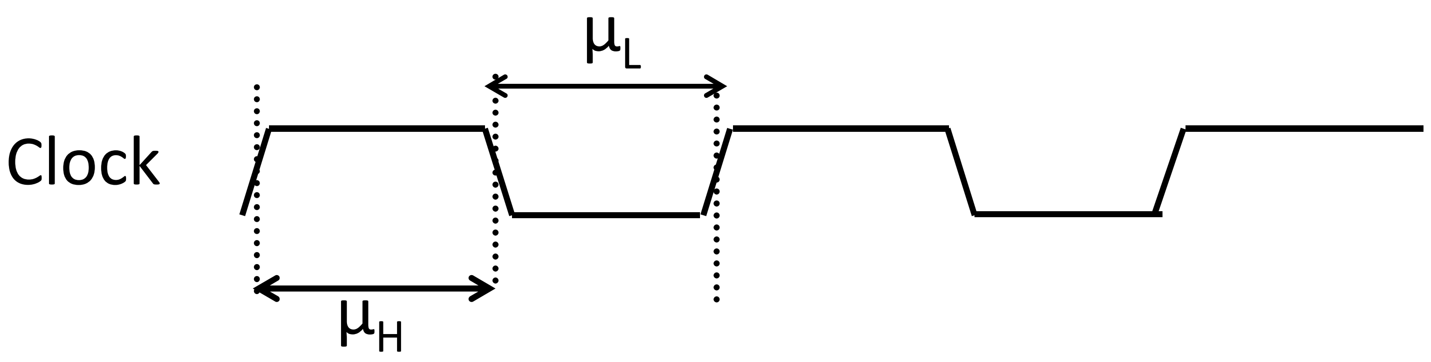
- Clock quality terminology
- Clocking architectures and circuits
  - Clock synthesizer
  - VCO
  - Clock distribution
  - Clock recovery
- Clock calibration
- Clock amortization and power management

Clock Non-Idealities



- Clock jitter/phase noise metrics are at the foundation of most industry specifications
- Crucial to analyzing and designing clock architectures
- Deviation of clock from an ideal edge
  - Skew is "static"
  - Jitter is "dynamic"

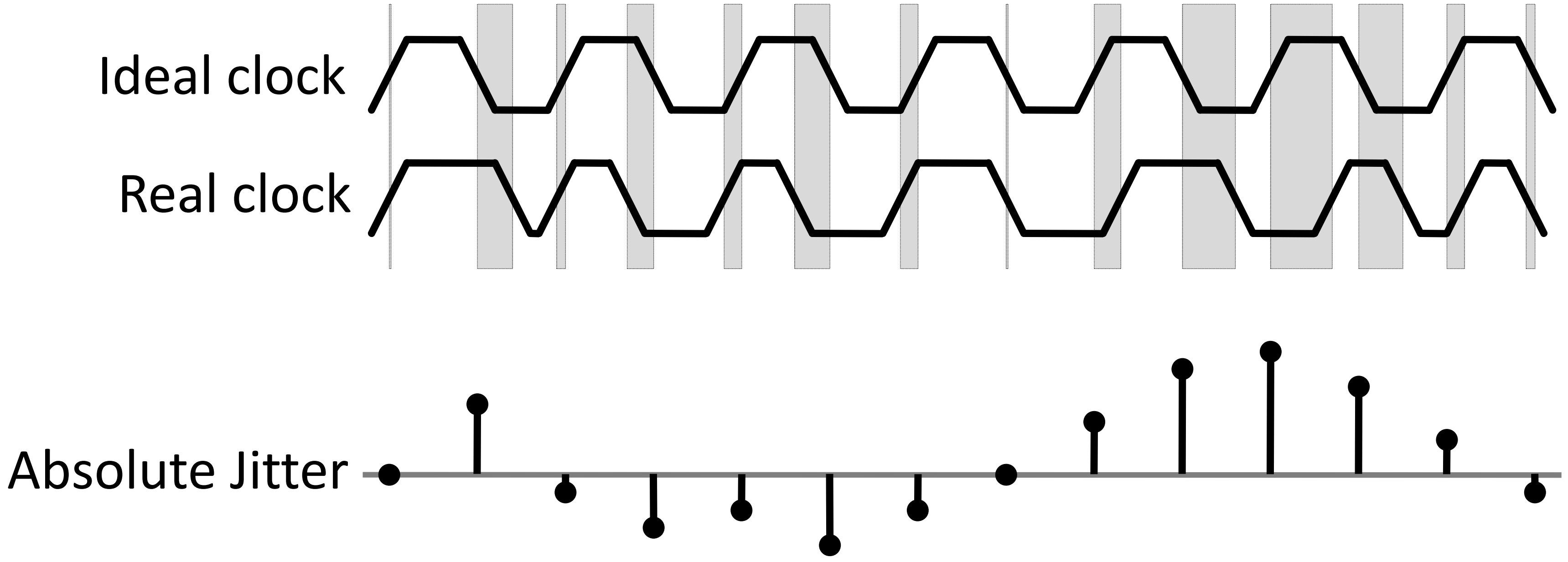
Clock Skew



$$DCE = \left|\frac{\bar{\mu}_H - \bar{\mu}_L}{2\bar{\mu}}\right|$$

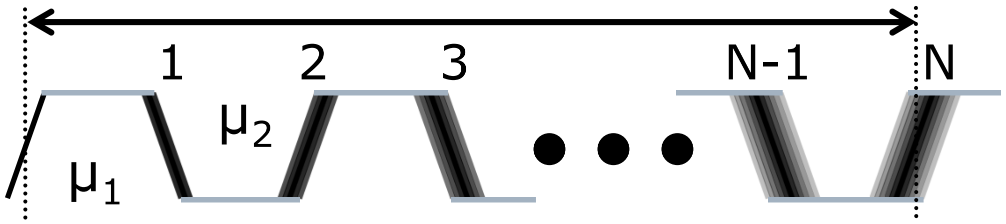
- Caused by process variation and design/layout imperfections
- Deterministic and can be detected/corrected
- Examples
  - Duty-cycle error (DCE)
  - Multi-phase clock such as quadrature error

Clock Jitter



- Jitter can be random or deterministic, due to
  - Device noise such as thermal and flicker noise (random)
  - Supply/substrate noise, channel induced jitter (deterministic)
- Frequency content of "Jitter" is better metric for clock quality
  - In many cases, much of the jitter may be tracked by the RX

Jitter Metrics



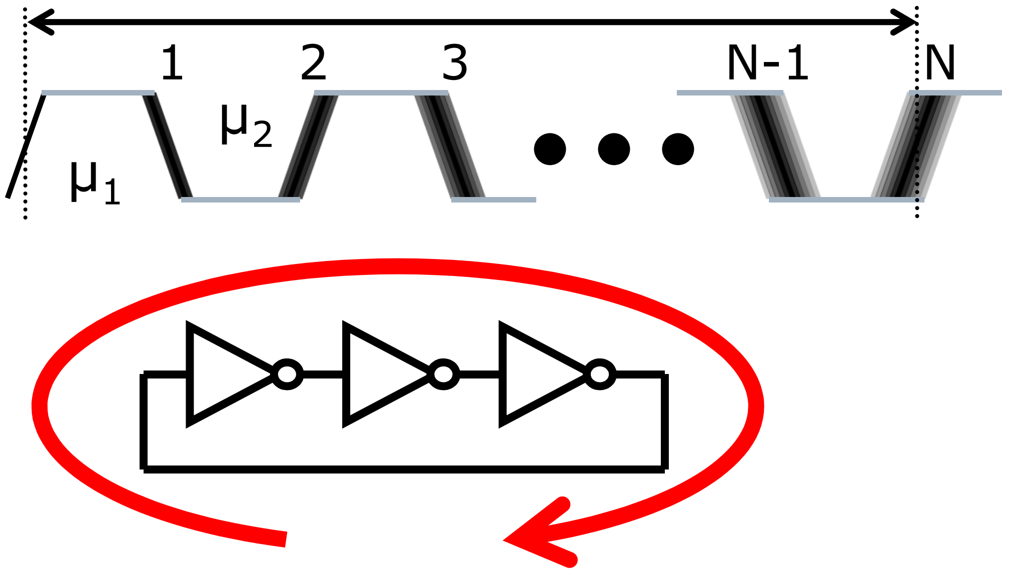
- Cycle jitter = $\mu_i - \overline{\mu}$
- Cycle-to-cycle jitter = $\mu_{i+1} - \mu_i$

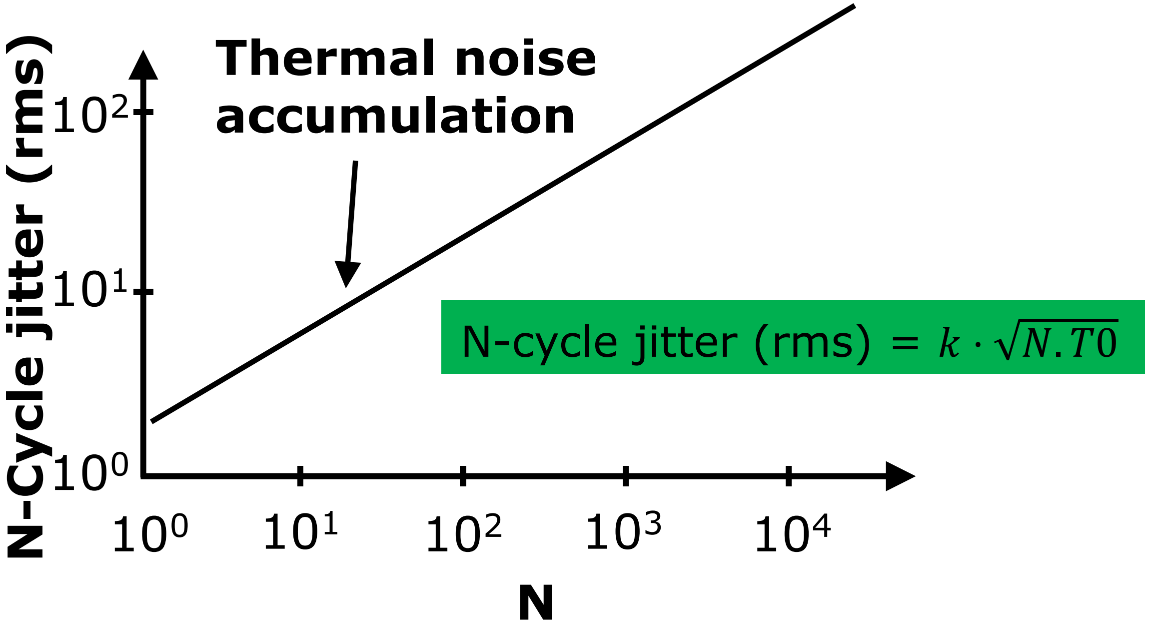
High frequency content of jitter

- N-cycle jitter = $\sum_{1}^{N} (\mu_i - \overline{\mu})$

Accumulation aspect of jitter

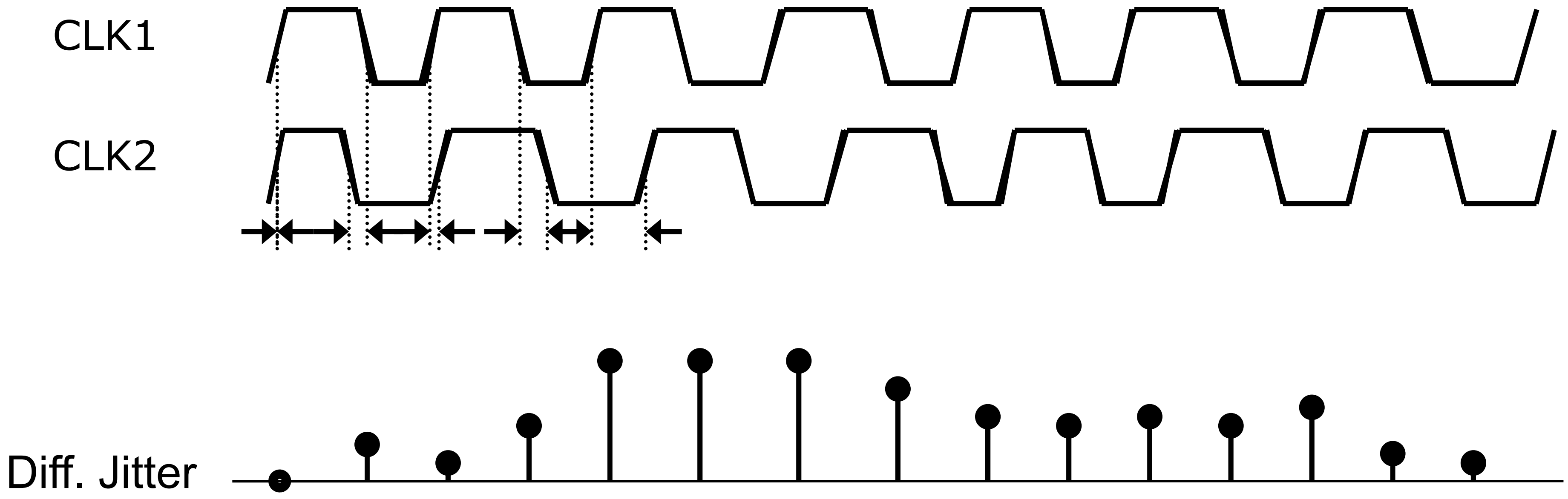
N-Cycle Jitter Example





- Free-running oscillator
  - Jitter accumulates as edge propagates circularly

Differential Jitter

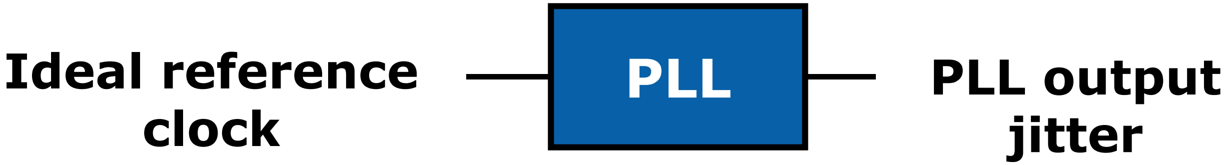


- Similar to absolute jitter, but with reference being another clock/data
- Example: forwarded clock (FC) applications
  - Clock-data jitter

System-Level Jitter Metrics

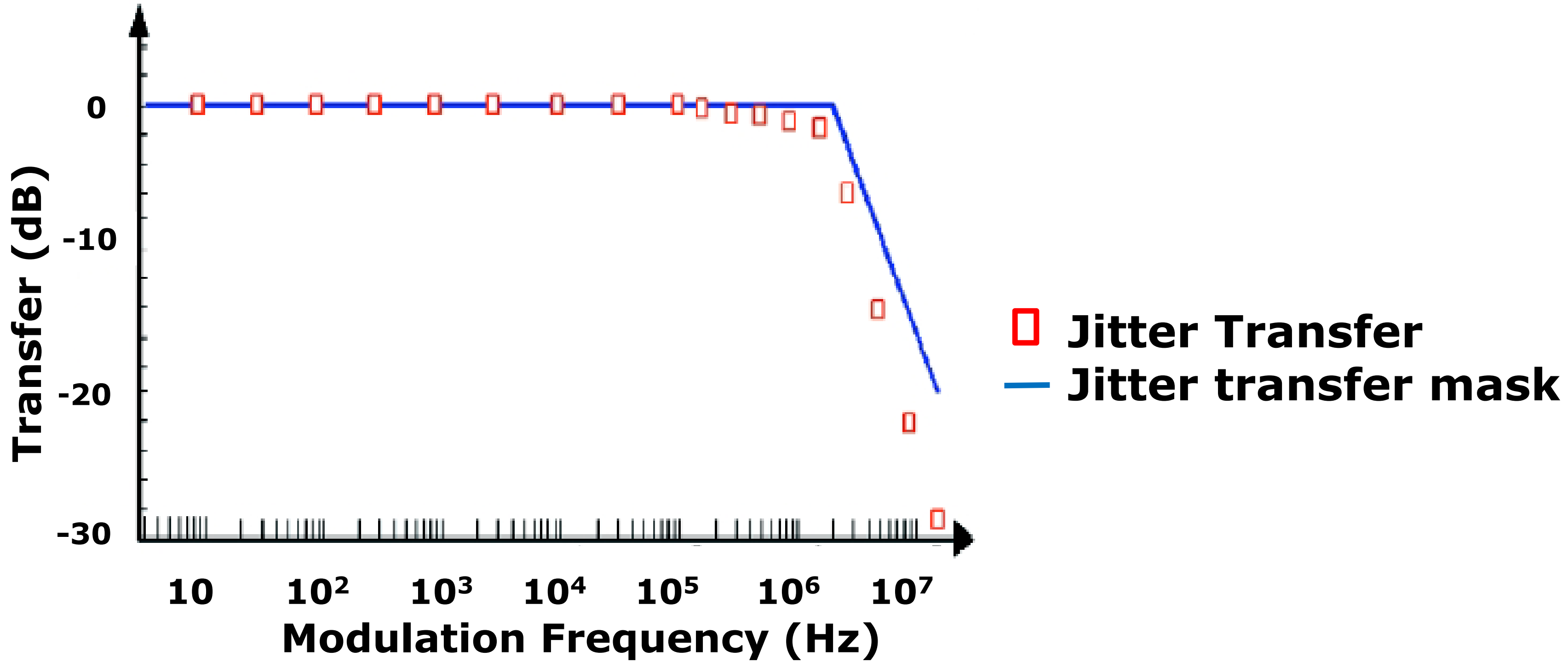
- Jitter generation
- Jitter transfer
- Jitter amplification
- Jitter tolerance

Jitter Generation



- Represents the intrinsic jitter at the output of a component when all other inputs are ideal
- Applicable to clock synthesizer and distribution
- A PLL example is shown

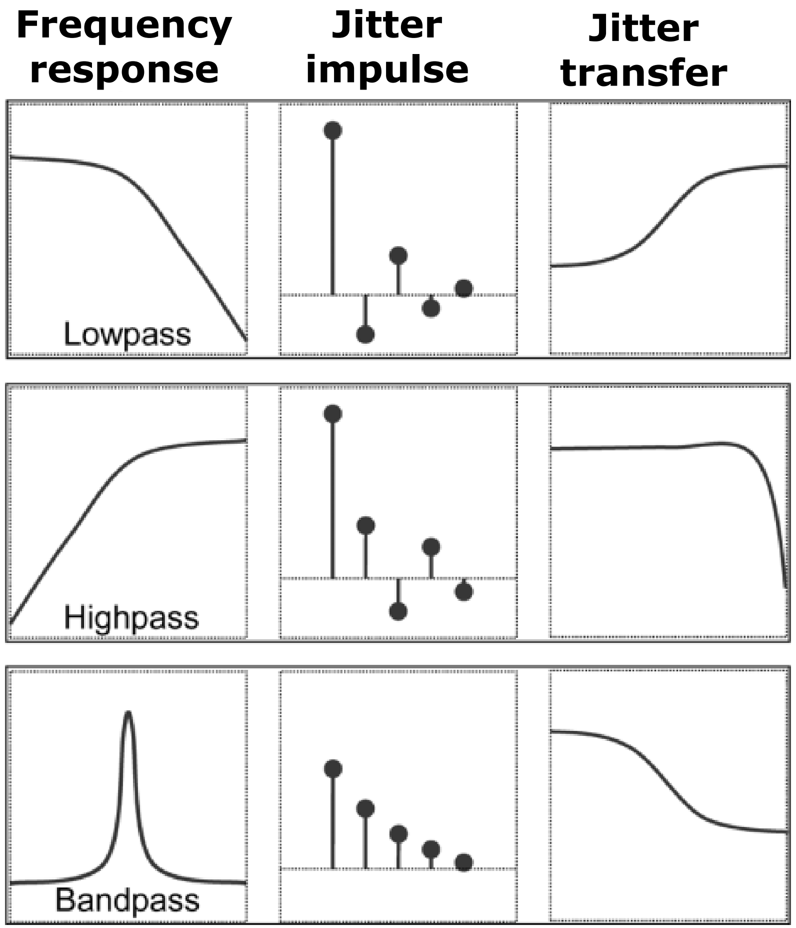
Jitter Transfer



- Represents how a component shapes the input jitter
  - Ratio of output to input jitter as a function of frequency
- Mask is representative of target/standard requirement

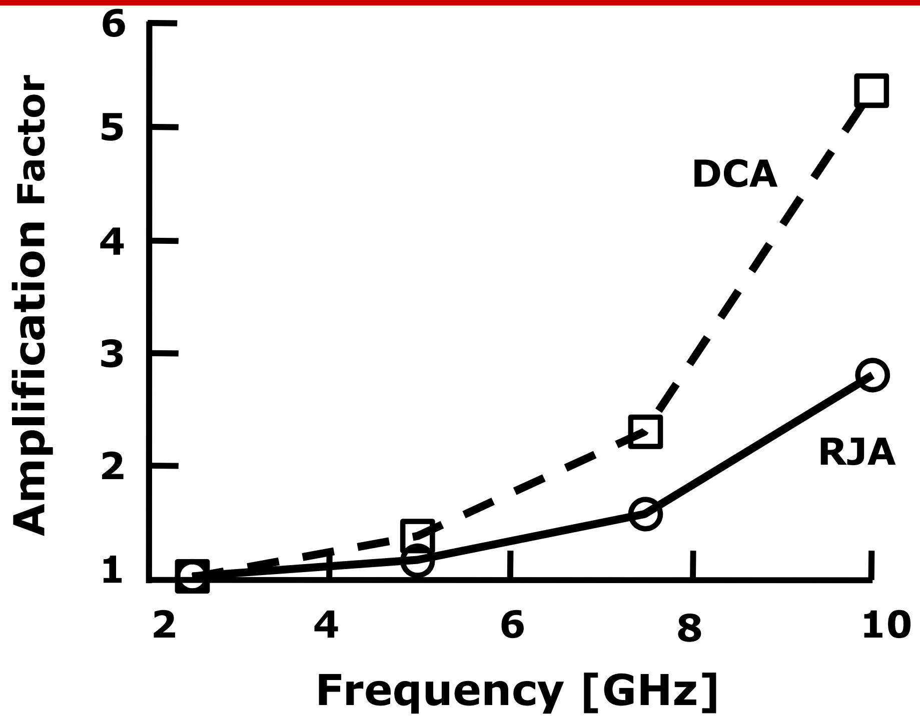
Jitter Transfer vs. Frequency Response

- A bandwidth limited clock component amplifies jitter at high frequencies
  - Examples: Buffer, clock distribution
- A high-pass system with a pole << clock frequency passes all frequencies of jitter
  - Example: AC-coupled system
- A band-pass system with the center frequency aligned with the fundamental clock frequency, filters high frequency jitter
  - Example: Clock resonant network



B. Casper et al., "Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links-A Tutorial," TCAS-I, Jan 2009.

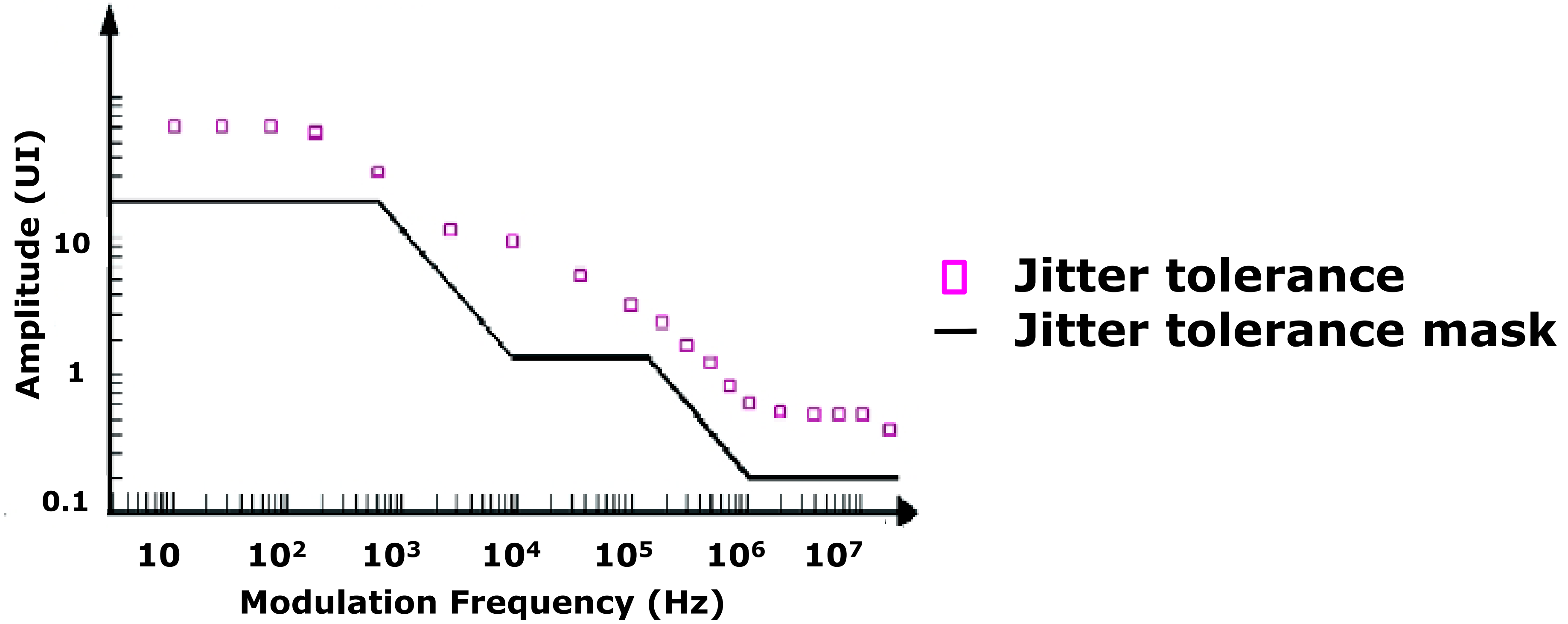
Jitter Amplification



B. Casper et al., "Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links-A Tutorial," TCAS-I, Jan 2009.

- Metric for bandwidth limitation of clock driver/distribution
  - Random jitter amplification (RJA) of input clock
  - Clock distribution signal integrity

Jitter Tolerance



- How well a receiver can tolerate input jitter
  - Achieving target bit error rate (BER) when subjecting the input to a sinusoidal phase modulated source at specified frequency and amplitude
- Mask is representative of target/standard requirement

Outline

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  - VCO
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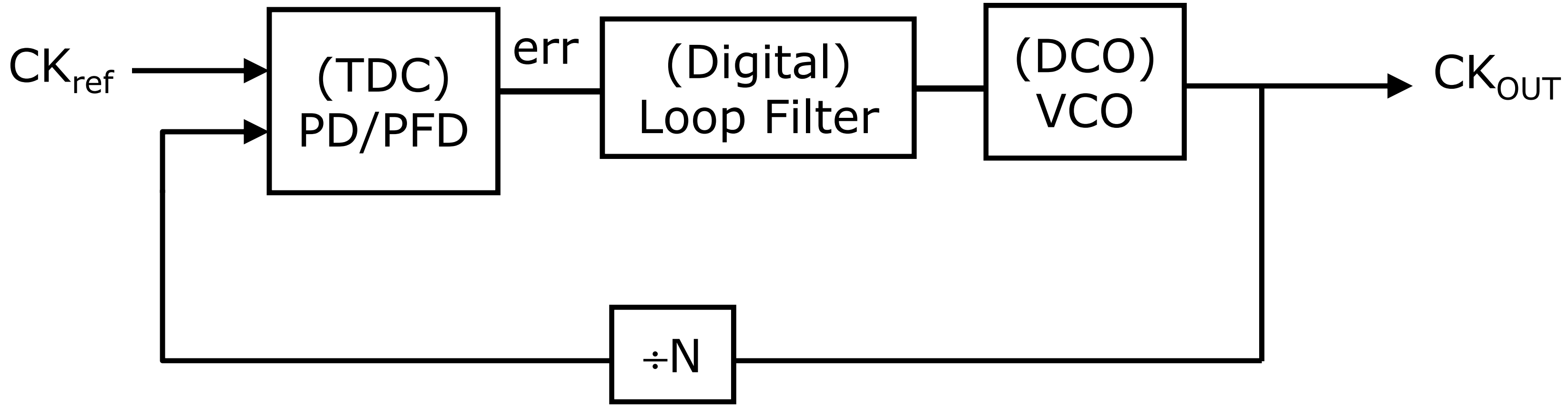
Clock Synthesizer Techniques

- Phase-locked loops (PLLs)
- Multiplying delay-locked loops (M-DLLs)
- Sub-sampling PLLs
- Sub-harmonic injection-locked oscillators (ILOs)

Phase-Locked Loops (PLLs)



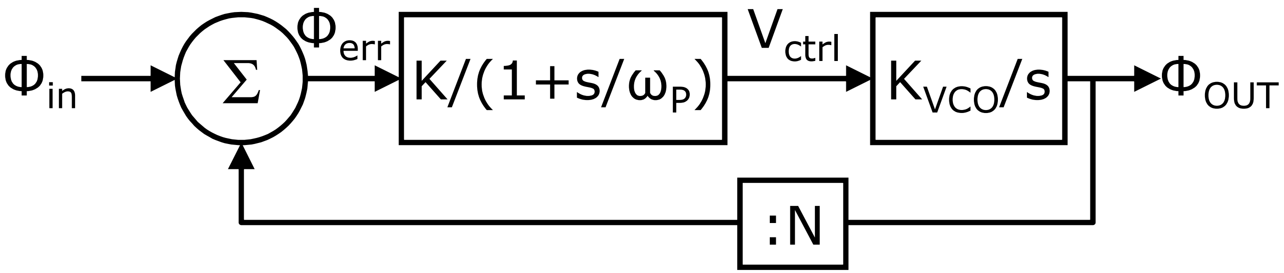
- PLLs multiply and filter external reference clock (Ck_{ref})
  - PD/PFD* compares Ck_{ref} with divided VCO** clock and produces an error signal
  - The error signal is low-pass filtered and drives the VCO
  - The negative feedback loop locks the VCO phase to the reference clock phase

* Phase detector (PD) or phase/frequency detector (PFD)
** Voltage-controlled oscillator (VCO)

PLL Loop Types

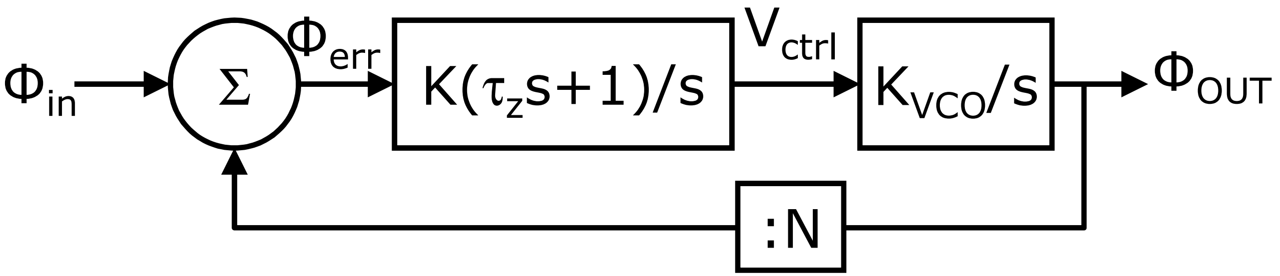
- Type I
  - Proportional (P) feedback
  - Static phase error
  - Unconditionally stable

Type I



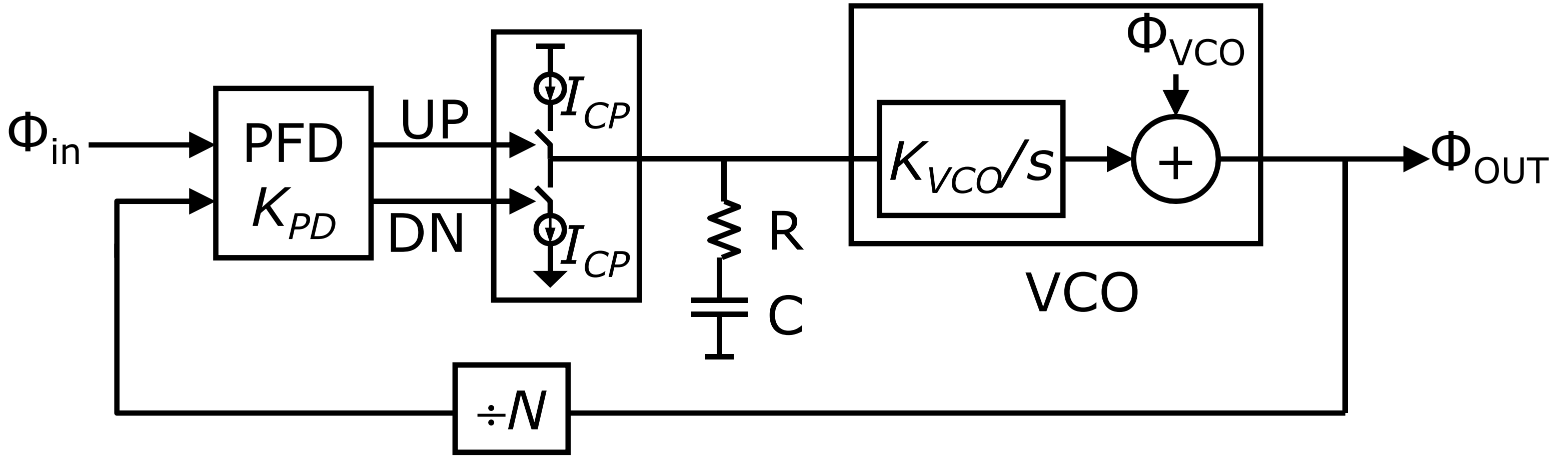
- Type II
  - Proportional-integral (P-I) feedback
  - No static phase error
  - 2 poles @ DC → requires stabilization

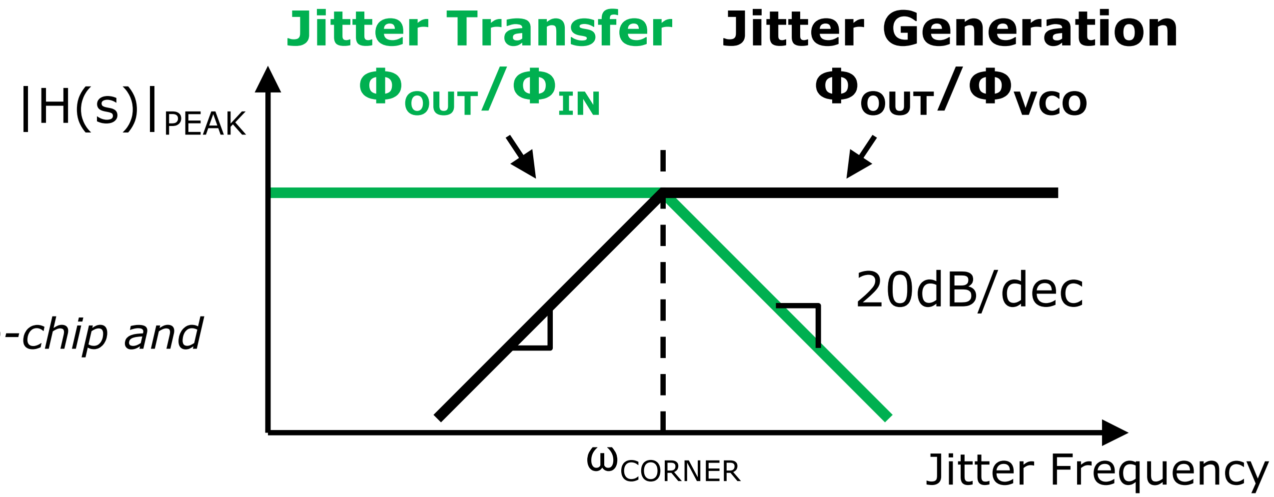
Type II



Type II PLL: Jitter Transfer & Generation

- PLL bandwidth tradeoffs
  - Lowering PLL bandwidth (BW) rejects input jitter
  - Increasing PLL BW rejects VCO jitter

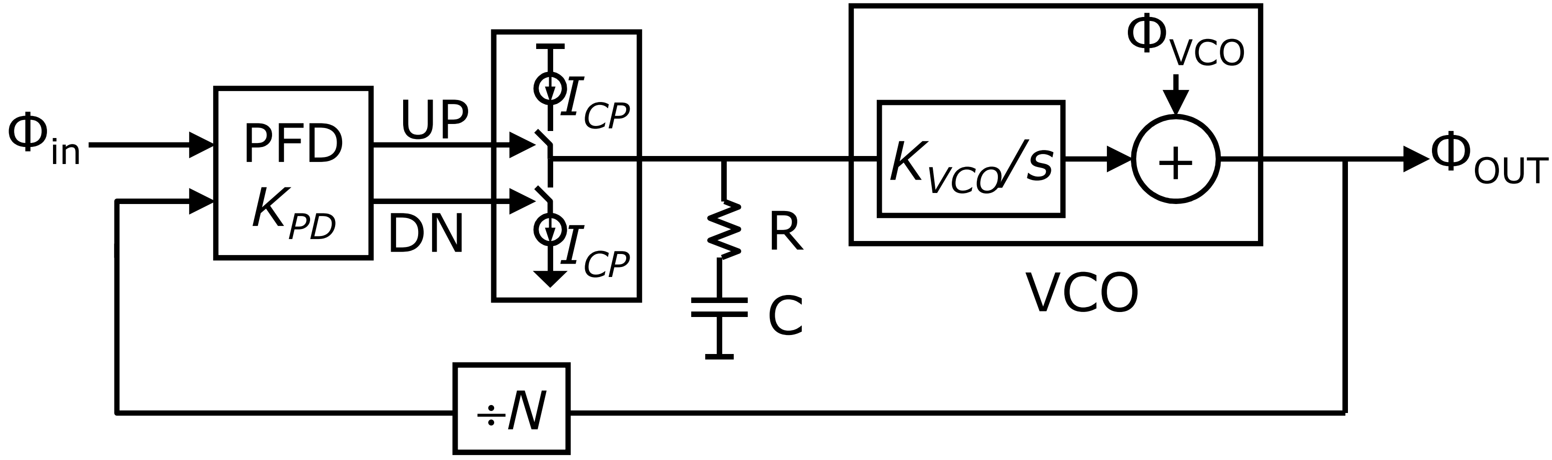


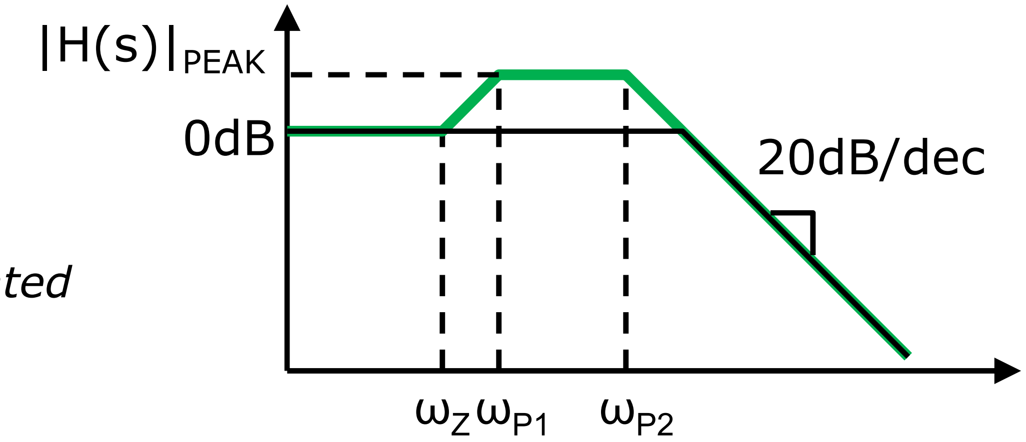


A. Sheikholeslami, "Basics of high-speed chip-to-chip and backplane signaling", ISSCC Tutorial 2008

Type II PLL: Closer look at Jitter Transfer

- Jitter transfer peaking is a function of zero and poles location
- Minimizing the peaking is desirable as it amplifies the input jitter





T. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998, p. 458.

PLL Jitter/Phase Noise Components

- Voltage-controlled oscillator (VCO)
- Input reference clock
- Divider
- Phase/frequency detector (PD/PFD)
- Charge-pump (CP)

VCO Jitter

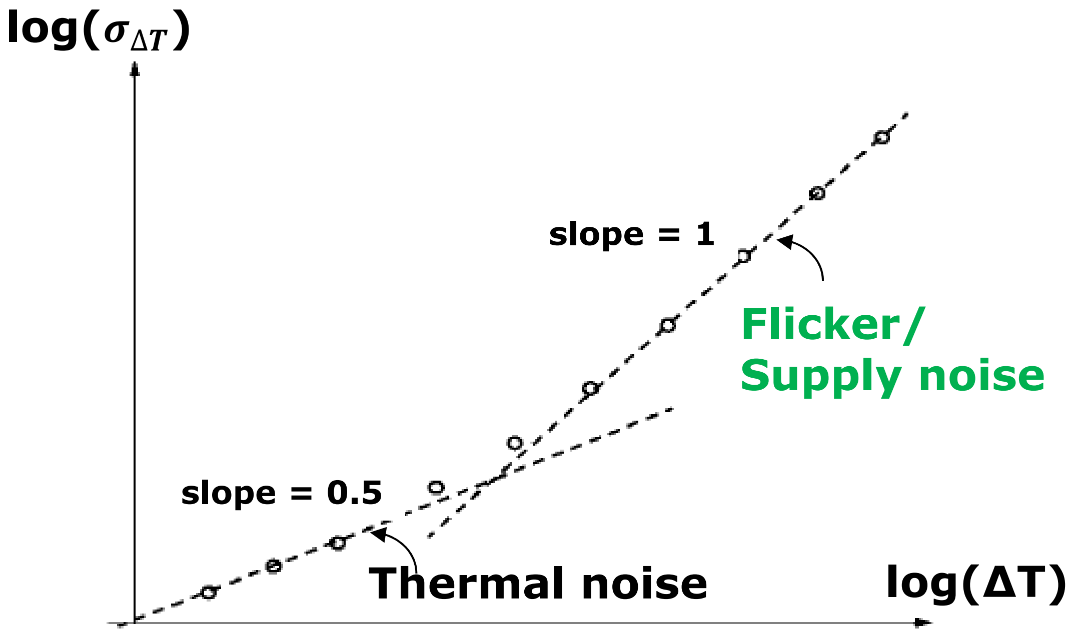
- Jitter accumulates as uncertainty in earlier transitions affects the following ones
  - Thermal noise is uncorrelated

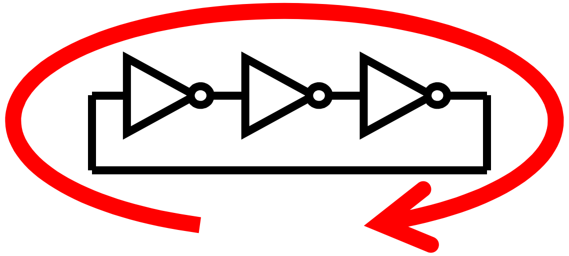
    $\sigma_{\Delta T} = k \cdot \sqrt{\Delta T}, \quad \Delta T = N.T0$

  - Flicker and supply noise induced jitter are correlated

    $\sigma_{\Delta T} = \delta \cdot \Delta T, \quad \Delta T = N.T0$

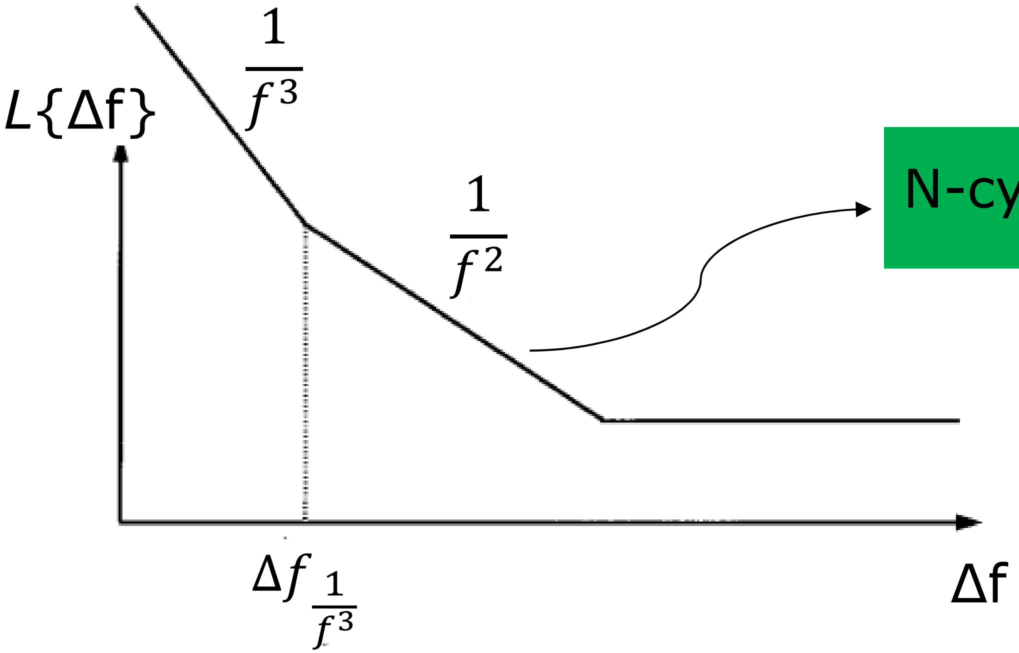
- κ and δ are determined by VCO design





A. Hajimiri et al., "Jitter and phase noise in ring oscillators," JSSC, June 1999

VCO Phase Noise

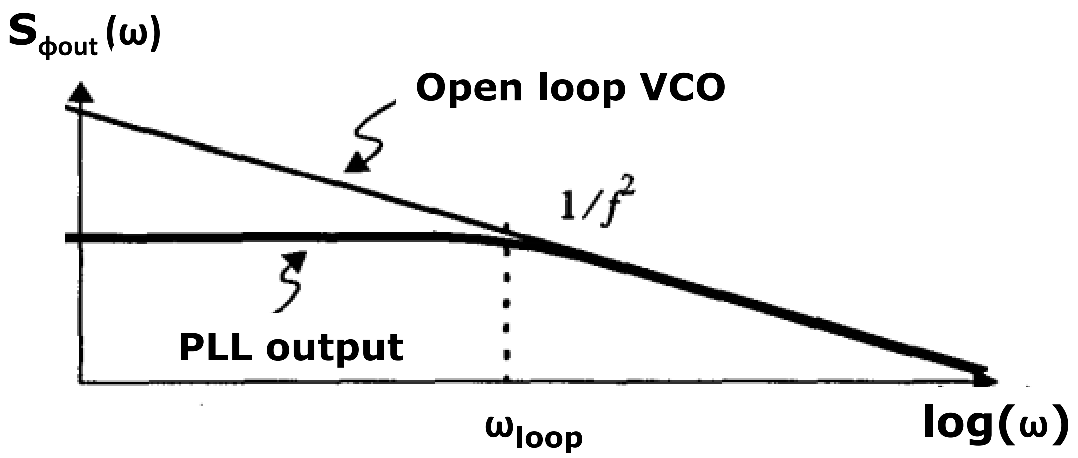


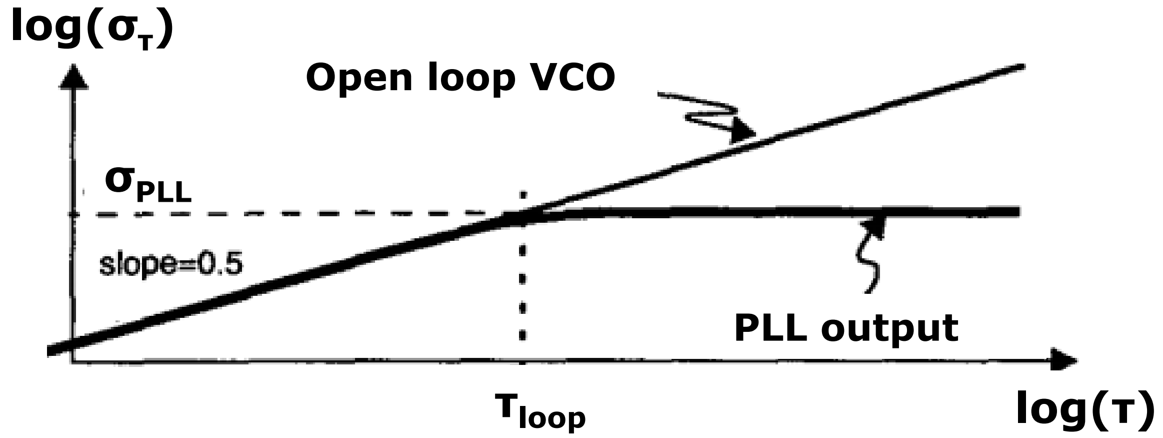
N-cycle jitter (rms) $= \frac{\Delta f}{f_o^{3/2}} \cdot 10^{\frac{L(\Delta f)}{20}} \cdot \sqrt{N}$

A. Hajimiri et al., "Jitter and phase noise in ring oscillators," JSSC, June 1999

- Phase noise metric is widely used in wireless/mmwave
- Convert phase noise to N-cycle jitter
  - Thermal noise dominated
  - No amplitude modulation

PLL Phase noise & Jitter: Noisy VCO

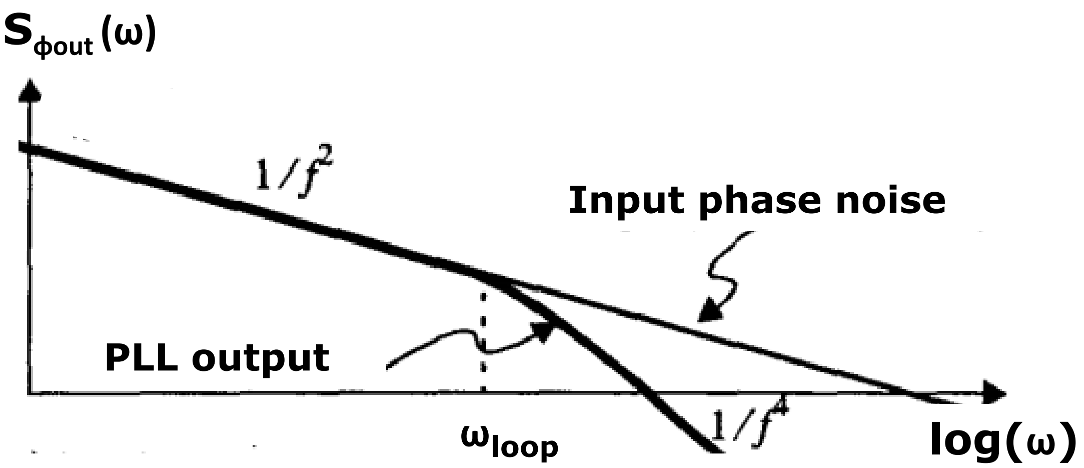


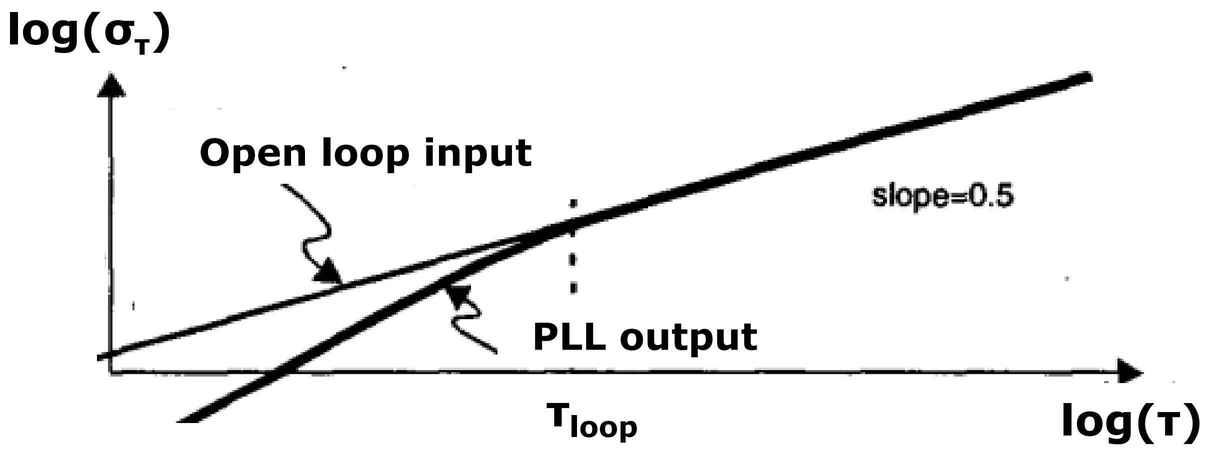


A. Hajimiri, "Noise in Phase-Locked Loops [Invited]," SSMSD, Feb. 2001

- Assuming an ideal input clock & 1st-order PLL
  - PLL filters the VCO phase noise for frequencies < PLL BW
  - Jitter accumulates up to PLL BW → The higher the BW, the lower the VCO jitter

PLL Phase noise & Jitter: Noisy Input

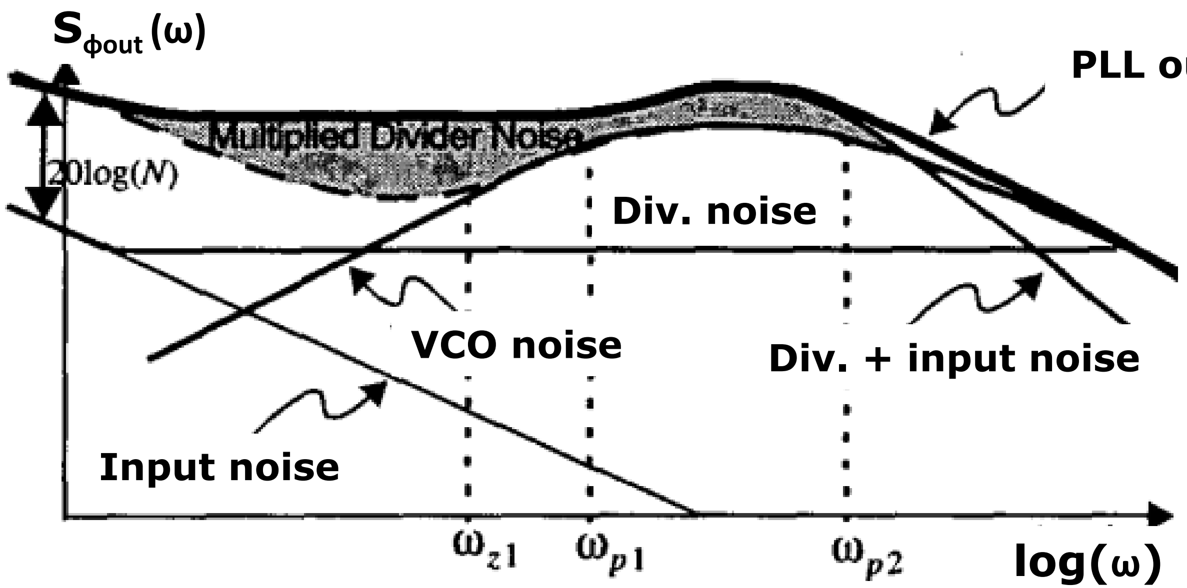




A. Hajimiri, "Noise in Phase-Locked Loops [Invited]," SSMSD, Feb. 2001

- Assuming an ideal VCO & 1st-order PLL
  - PLL filters the input phase noise for frequencies outside PLL BW

Impact of Divider on PLL Phase noise



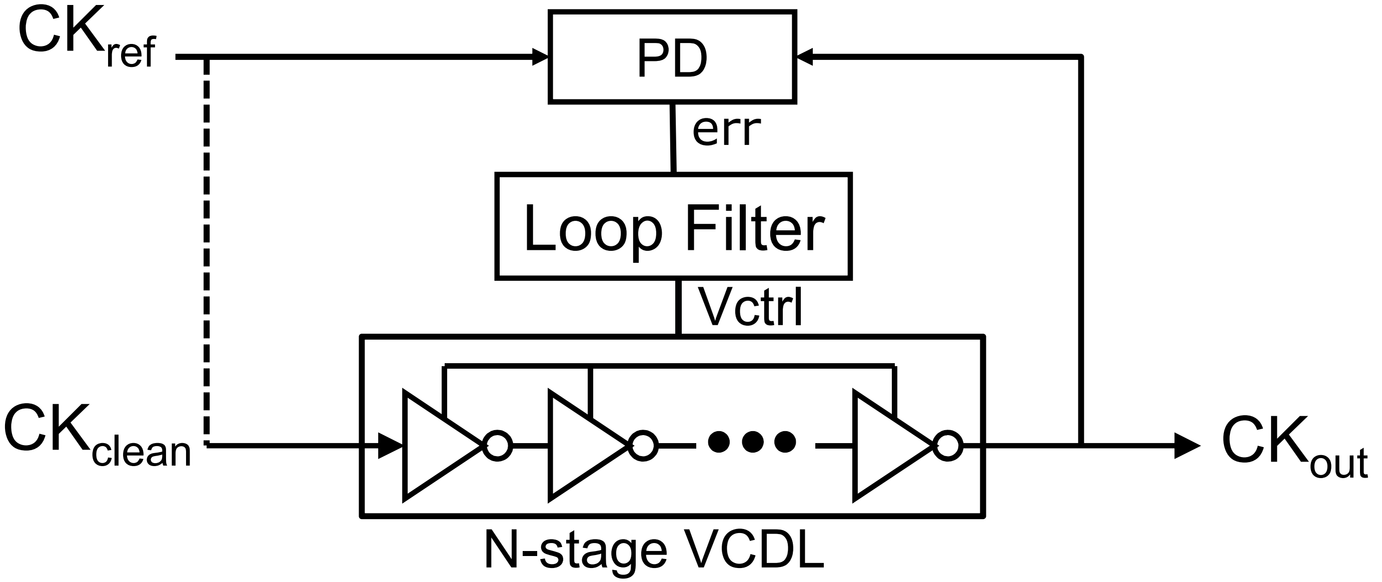
A. *Hajimiri, "Noise in Phase-Locked Loops [Invited],"* SSMSD, Feb. 2001

- An ideal frequency divider increases
  - Input phase noise (by 20log(N))
  - Charge-pump/phase detector phase noise (by 20log(N))
- Divider white noise adds to the input noise

Clock Synthesizer Techniques

- Phase-locked loops (PLLs)
- Multiplying delay-locked loops (M-DLLs)
- Sub-sampling PLLs
- Sub-harmonic injection-locked oscillators (ILOs)

Delay-Locked Loops (DLLs)

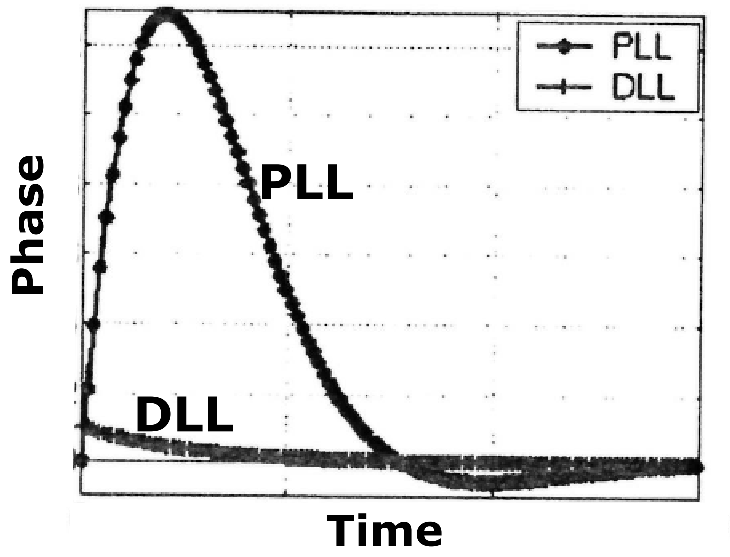


- Similar to PLL
  - PD compares reference clock and voltage-controlled delay line (VCDL) output clock and produces an error signal
  - The error signal is low-pass filtered to control the delay of N-stage VCDL
- VCDL input can be either a reference clock or a clean clock signal

DLL vs. PLL

- ☑ Unlike VCO, VCDL does not accumulate jitter
- ☑ DLL is unconditionally stable
- ☑ Loop filter can be an integrator or accumulator
- ☒ No filtering on input clock
  - ❑ Requires an additional clean clock
- ☒ False lock to harmonics
- ☐ Multiplication?

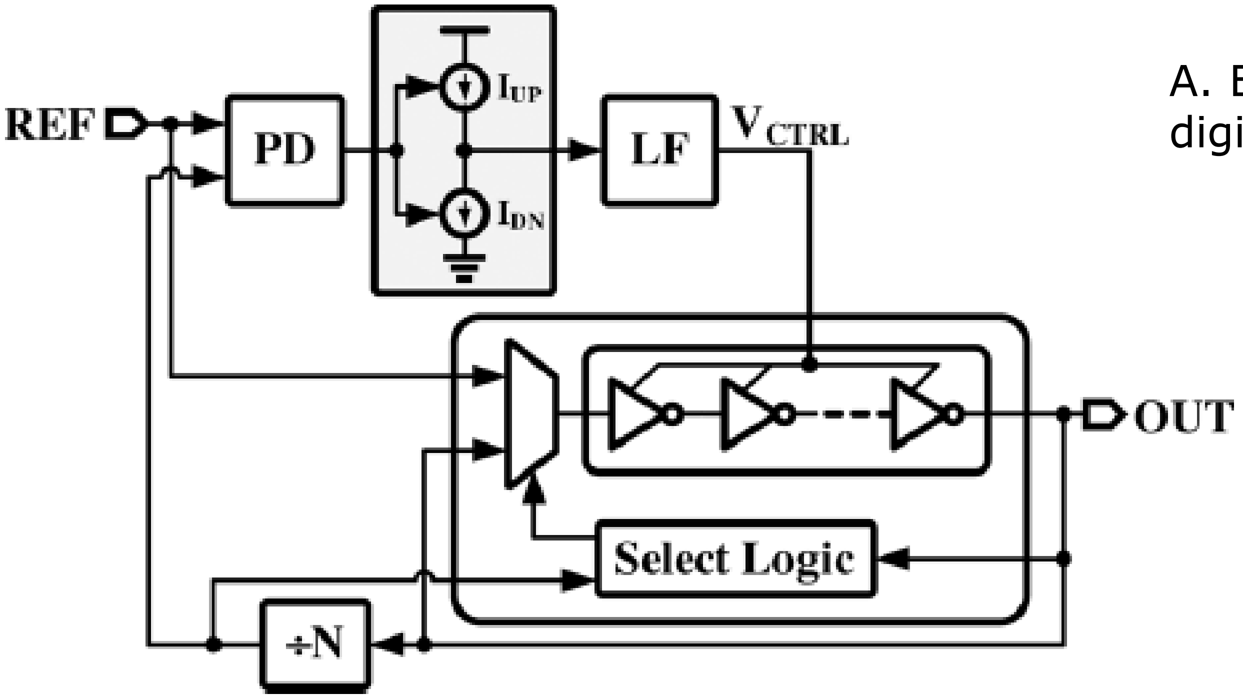
Phase response to step



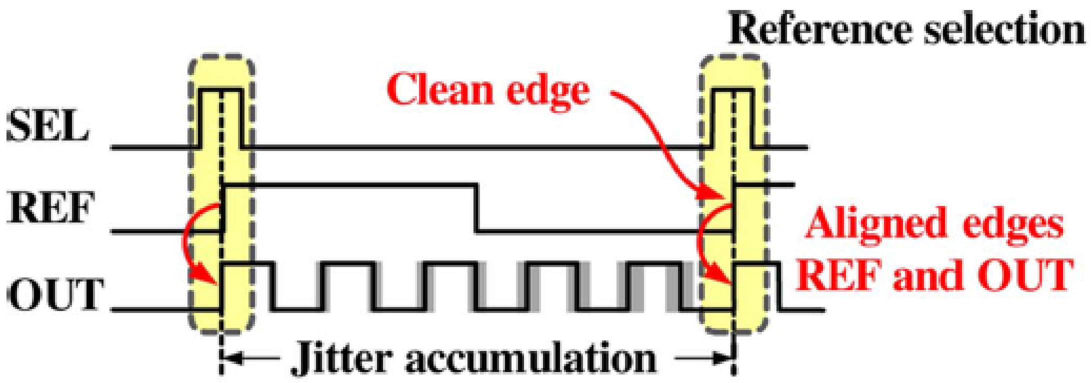
- ❑ **PLL and DLL**
  - ➢ **Same BW**
  - ➢ **Same delay elements**
- ❑ **PLL is 2nd-order with ζ=1**

B. Razavi, Phase locking in high-performance systems Wiley-IEEE Press Press, 2003.

Multiplying DLL



A. Elshazly et al., "Clock multiplication techniques using digital multiplying delay-locked loops," JSSC 2013.



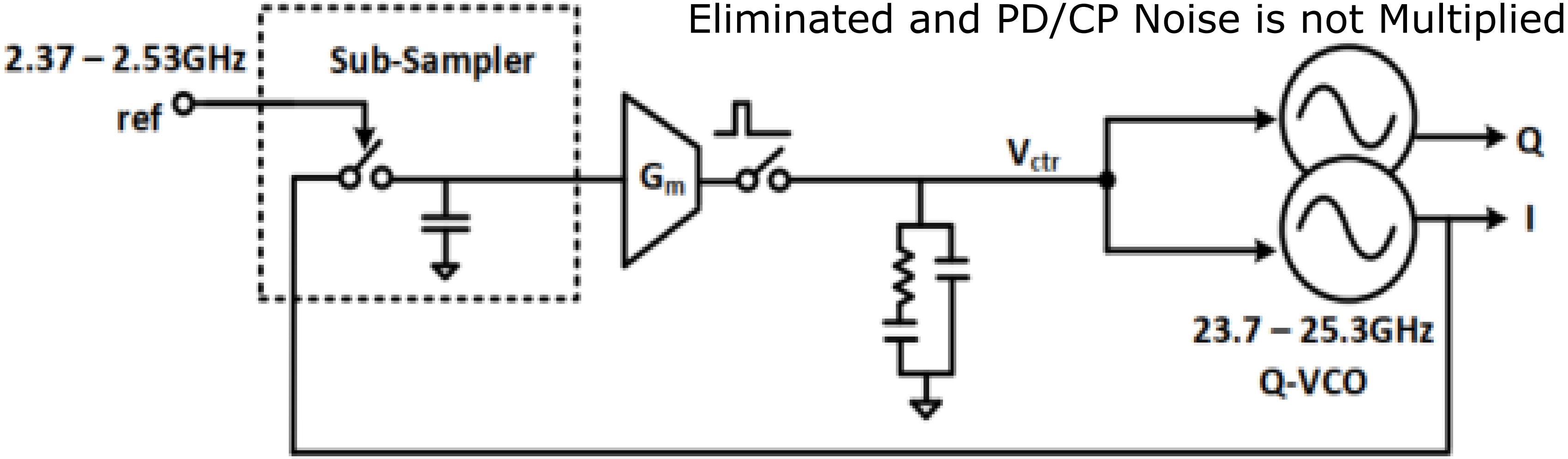
- Generates a phase-locked output clock at a multiple of the reference clock
- At every reference cycle, accumulated jitter of output clock is reset

Clock Synthesizer Techniques

- Phase-locked loops (PLLs)
- Multiplying delay-locked loops (M-DLLs)
- Sub-sampling PLLs
- Sub-harmonic injection-locked oscillators (ILOs)

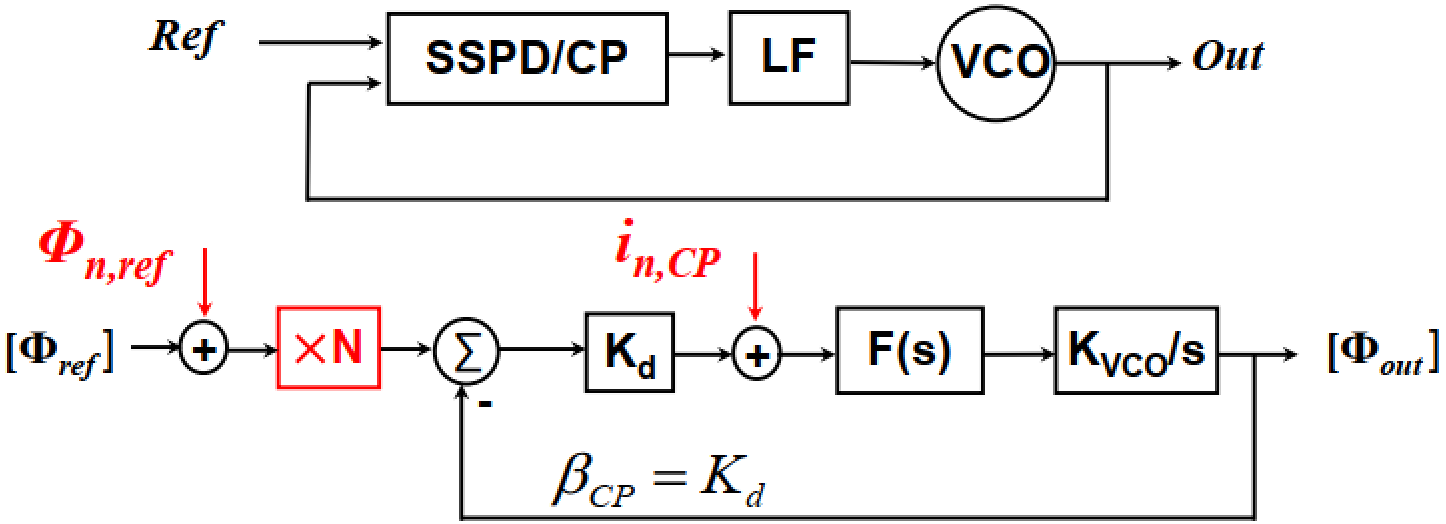
Sub-Sampling PLL

X. Gao et al., "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is not Multiplied by N^2," *JSSC*, Dec. 2009



- Sub-sampling VCO by a reference clock (no divider)
- Direct sampling of VCO output (no high-frequency/mmwave buffer)
- Phase/timing error converted into voltage error

Sub-Sampling vs. Classical PLL



- ❑ "Ref" phase noise increases by 20log(N) due to virtual multiplier, same as a PLL
- ☑ Charge pump (CP) phase noise is suppressed (no divider)
- ☑ Higher PLL BW and better VCO phase noise suppression
- ☒ May lock to harmonics
  - ☑ Can be addressed by frequency locked loop
- ☒ Larger capacitor due to high phase detection gain

Clock Synthesizer Techniques

- Phase-locked loops (PLLs)
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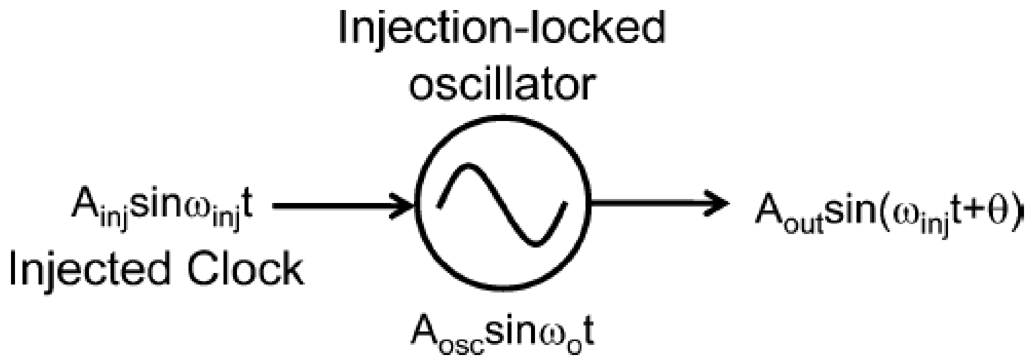
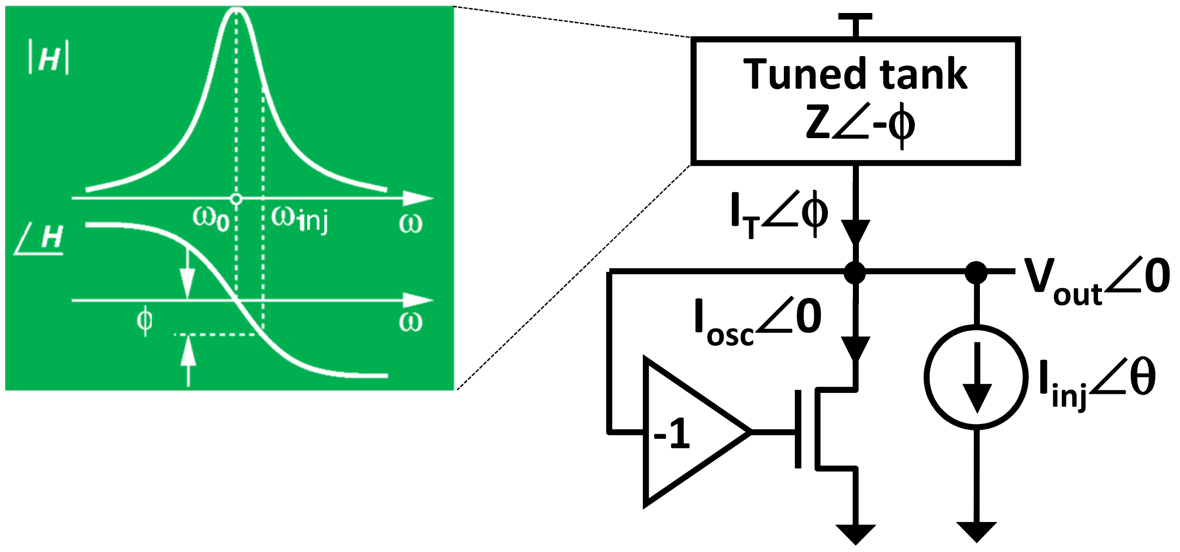
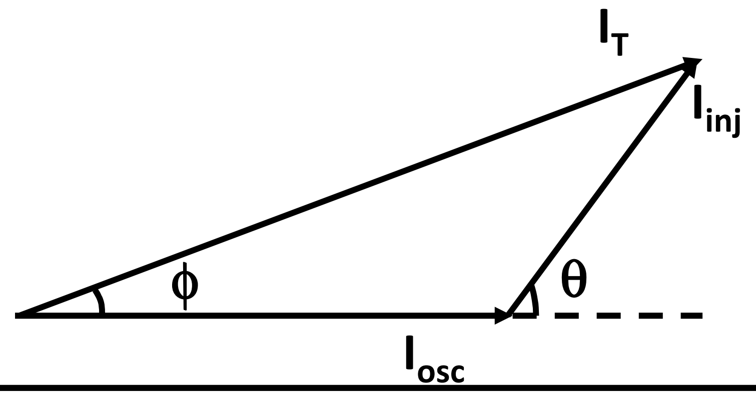
Injection-Locked Oscillators (ILOs)



- Locks to injected clock (within its lock range)
- 1st-harmonic ILO (f_{inj} = fo)
- Sub-harmonic ILO (f_{inj} = fo/N)
  - Frequency multiplier, similar to PLL/MDLL
  - False lock, similar to sub-sampling PLL/MDLL
- Behaves like a type-I PLL
  - Frequency mismatch causes phase offset

Injection Locking Theory





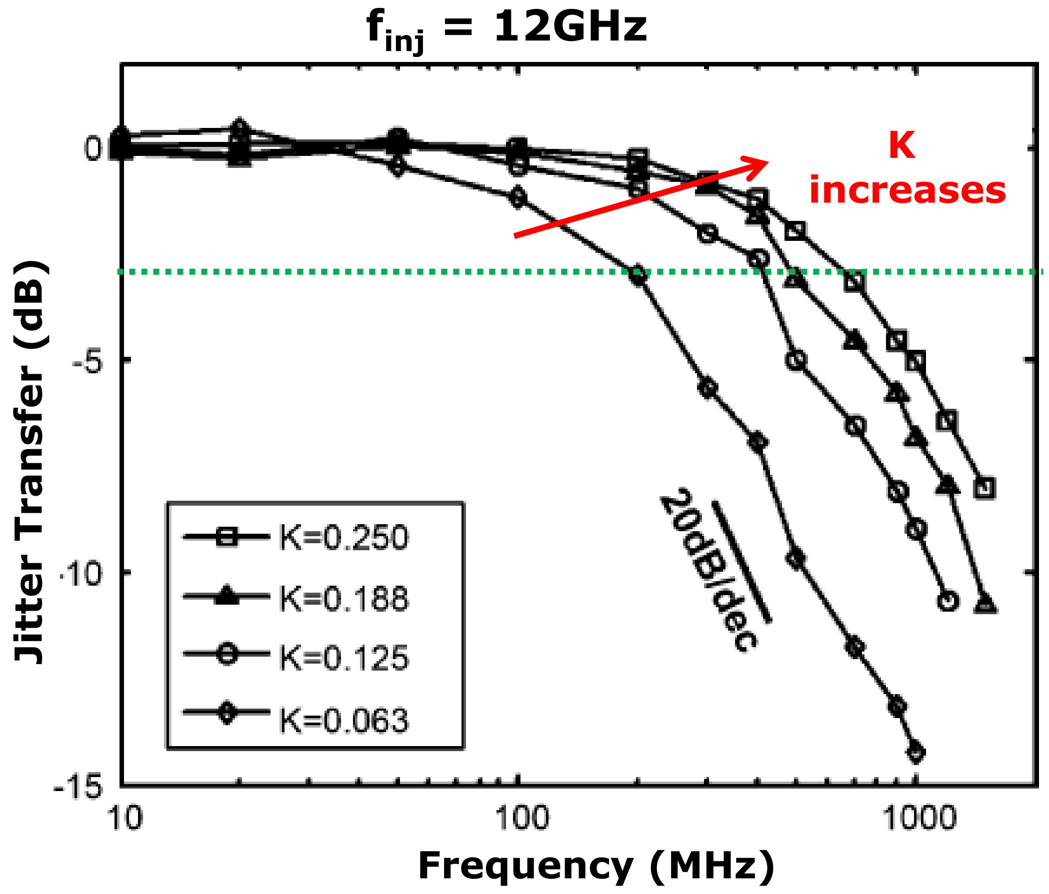
$$\tan\phi = \frac{I_{inj}\cdot\sin\theta}{I_{osc}+I_{inj}\cdot\cos\theta} = \frac{K\cdot\sin\theta}{1+K\cdot\cos\theta}, \quad K = \frac{I_{inj}}{I_{osc}}$$

K is injection strength

- Phase offset between injection and output clock if $\omega_{inj} \neq \omega_0$
- BW = $\frac{f_0}{2Q}\frac{K}{K+1}$ (for $f_{inj}=f_0$)
  - Bandwidth increases with K and reduces with Q

ILO vs. PLL

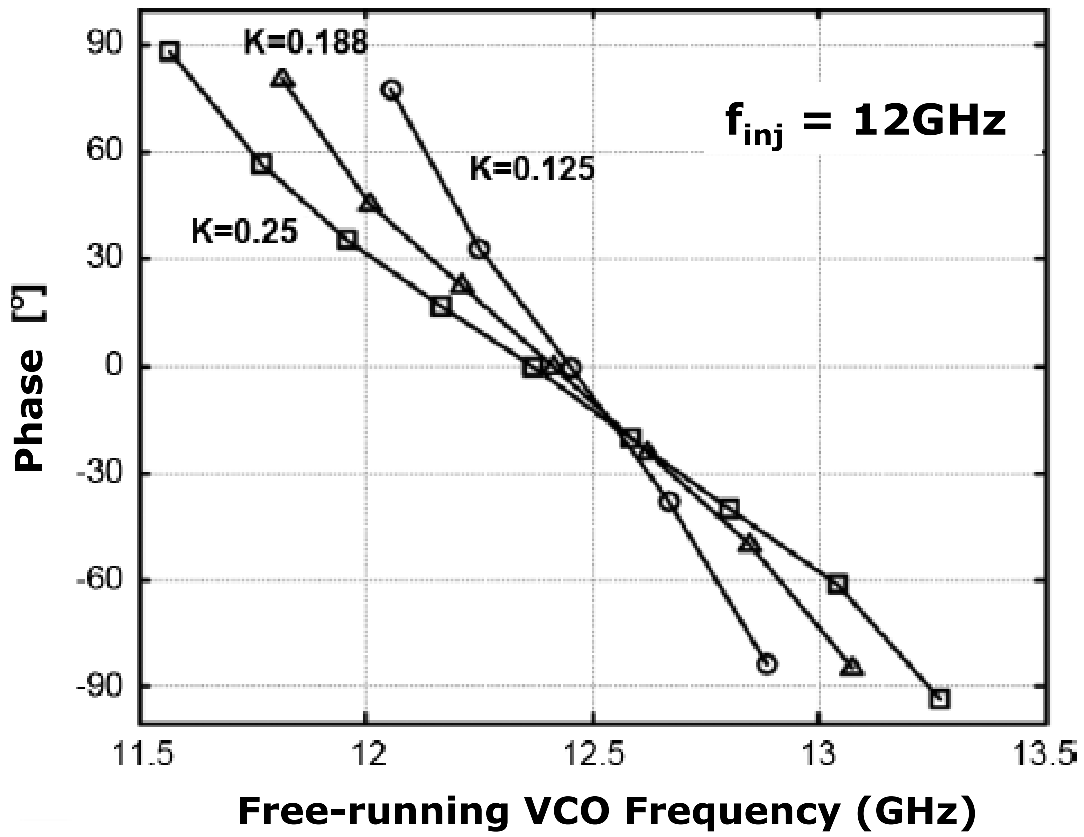
- ❑ 1^{st}-harmonic ILO
  - ☑ Can achieve higher BW and thus, better VCO noise performance
  - ☑ Low-bandwidth loop to set $f_0 = f_{inj}$
- ❑ Sub-harmonic ILO
  - ❑ Harmonic generation results in lower K and thus lower BW
  - ☒ A PLL to set $f_0 = N * f_{inj}$
- ☑ Phase rotation in clock recovery applications



S. Shekhar, et al., "Strong injection locking in low-Q LC oscillators: modeling and application in a forwarded-clock I/O receiver," JSSC 2009

ILO-Based Phase Rotation

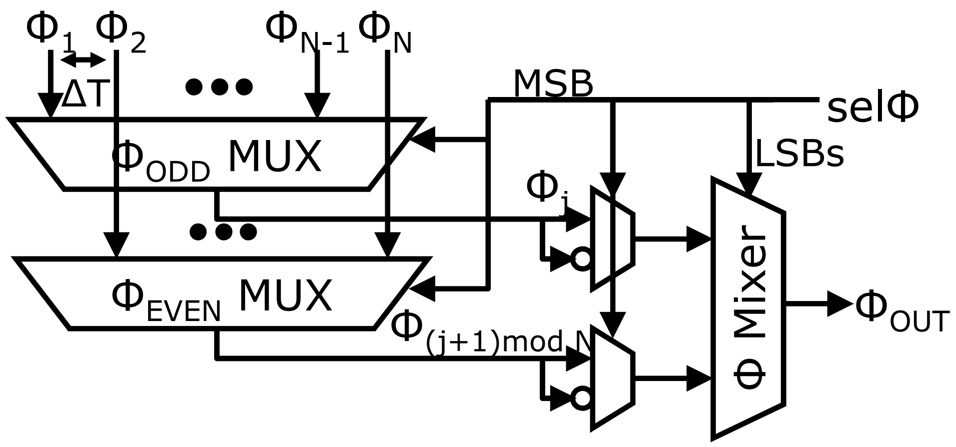
- ILO can recover and rotate the clock phase
  - Clock recovery sets VCO free-running frequency and thus rotates the phase
- Phase resolution and linearity vs. VCO tuning range
  - The higher the K, the better linearity/resolution
  - The lower the K, the smaller the tuning range

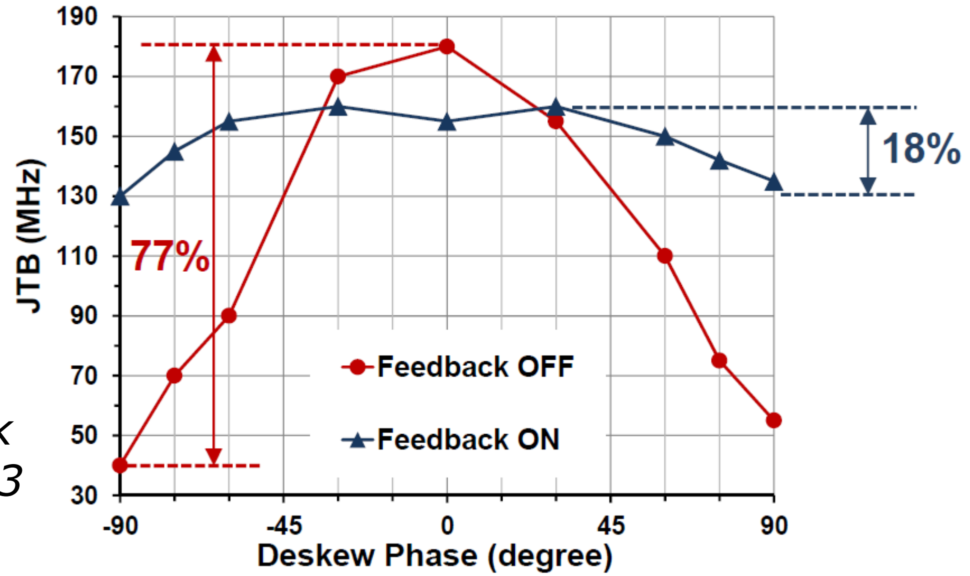


S. Shekhar, et al., "Strong injection locking in low-Q LC oscillators: modeling and application in a forwarded-clock I/O receiver," JSSC 2009

ILO-Based vs. Conv. Phase Interpolator

- ☑ Rotating the clock by tuning VCO frequency
  - ☑ No need for multi-phase generation or MUX
  - ☑ Low power and low area
- ☒ Limited vs. full phase rotation in PI
- ☒ BW varies with phase shift (Max BW @ phase = 0)
  - ☑ Dual feedback to reduce BW variation





J-H Seol, et al. "An 8Gb/s 0.65mW/Gb/s forwarded-clock receiver using an ILO with dual feedback …," ISSCC 2013

Clock Synthesizer Summary

- Generate a low-jitter multi-GHz clock from a low-frequency reference clock
  - Design tradeoffs between jitter transfer & jitter generation
- M-DLLs and ILOs are alternatives to PLLs
  - Lower jitter accumulation benefit
- Sub-sampling PLLs are widely used in wireless applications
  - Lower phase noise by suppressing CP/PD and eliminating divider phase noise
- ILO is an alternative to conventional PI for clock phase rotator

Outline

- Clock quality terminology
- Clocking architectures and circuits
  - Clock synthesizer
  - VCO
  - Clock distribution
  - Clock recovery
- Clock calibration
- Clock amortization and power management

Voltage Controlled Oscillators (VCOs)

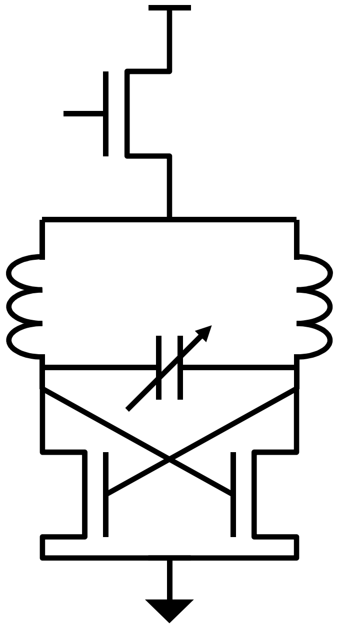
- Jitter/phase noise performance
- Supply noise sensitivity
- Operating frequency
- Tuning range
- Power
- Area

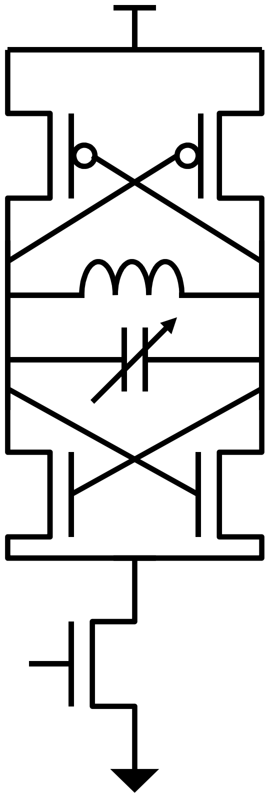
VCO Topologies

- LC-VCO
- Current-mode logic (CML) based VCO
- Inverter-based VCO

LC-VCO

- ☑ Excellent jitter/phase noise performance
  - ☒ Process support for integrated inductor
  - ☒ Lower Q in CMOS digital process
- ☑ Low supply noise sensitivity
- ☒ Large area due to passives
- ☒ Narrow frequency tuning range
- ☒ Portability challenges

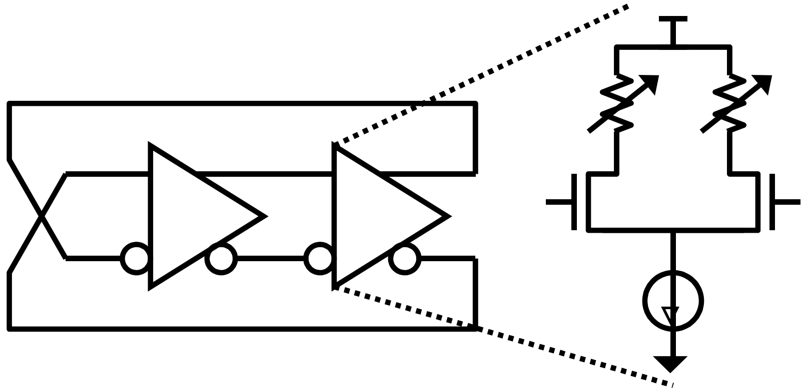




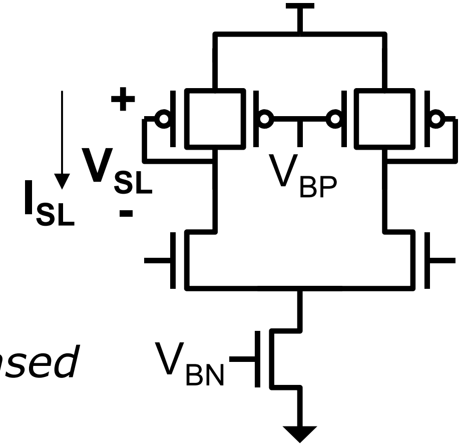
- **Different LC VCO topologies**
  - **Colpitts oscillator, quadrature LC-VCO, etc**

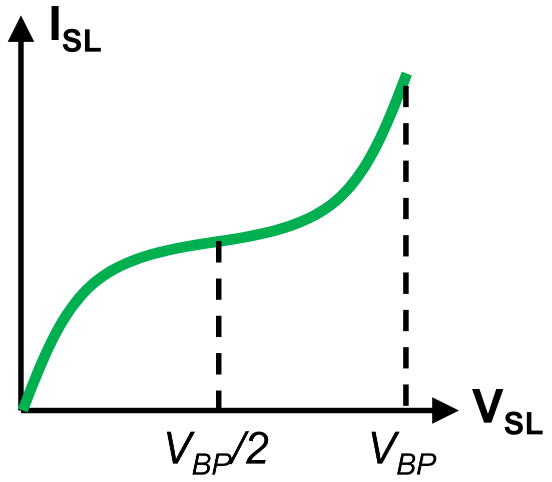
CML-Based VCO

- ☑ Wide frequency tuning range
- ☑ Power vs. frequency scaling
- ☑ Portable
- ☒ Poor jitter performance
- ☒ High bias/supply noise sensitivity



"Symmetric-Load" (SL) delay cell

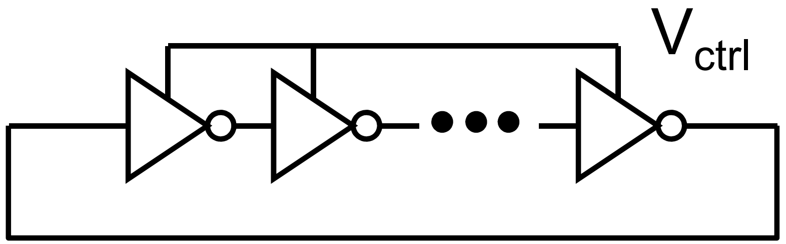


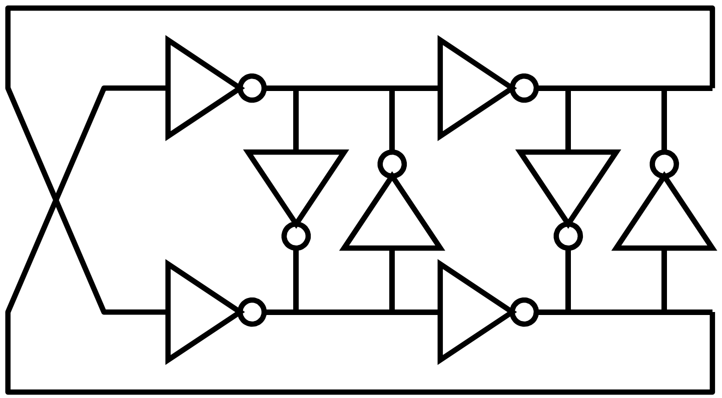


J. Maneatis, "Low-jitter process-independent DLL and PLL based self-biased techniques", JSSC, pp. 1723-1732, Nov. 1996

Inverter-Based VCO

- ☑ Wide frequency tuning range
- ☑ Power vs. frequency scaling
- ☑ Portable
- ☑ More variation-tolerant than CML-based
- ☐ Jitter performance
  - ☑ Better than CML-based
  - ☒ Worse than LC-VCO
- ☒ High supply noise sensitivity



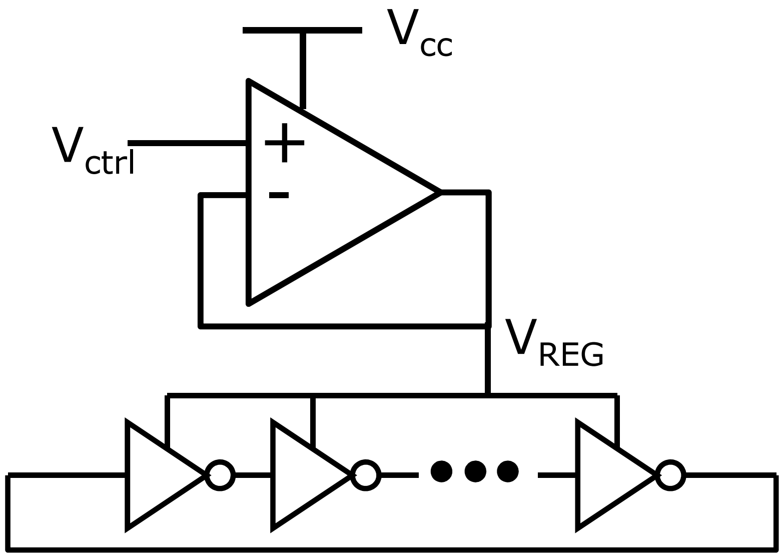


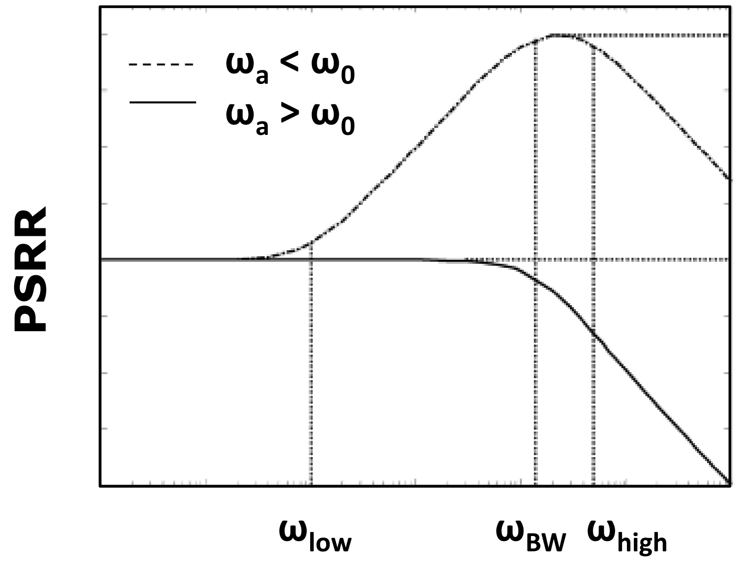
- **Variants on CMOS delay cells**
  - **Current, capacitively or digitally controlled**

VCO Comparison Summary

	Inv-Based VCO	CML-Based VCO	LC VCO
Jitter/ Phase Noise	2nd best	X	✓Best
Supply noise sensitivity	X needs regulator	2nd best	✓Best
Frequency range	✓Wide	✓Wide	X Narrow
Area	X Including regulator	✓Yes	X
Portable	✓Yes	✓Yes	X No

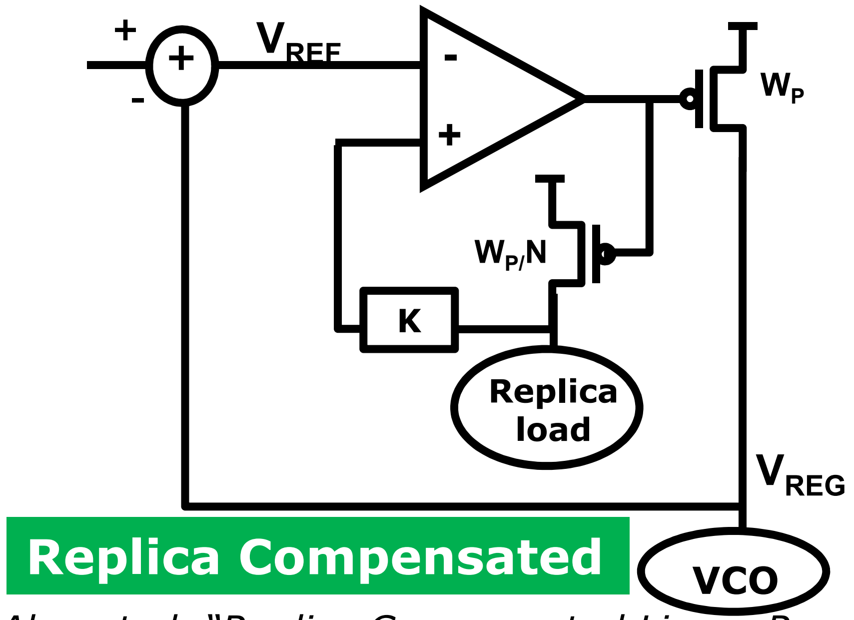
Regulated Inverter-Based VCO



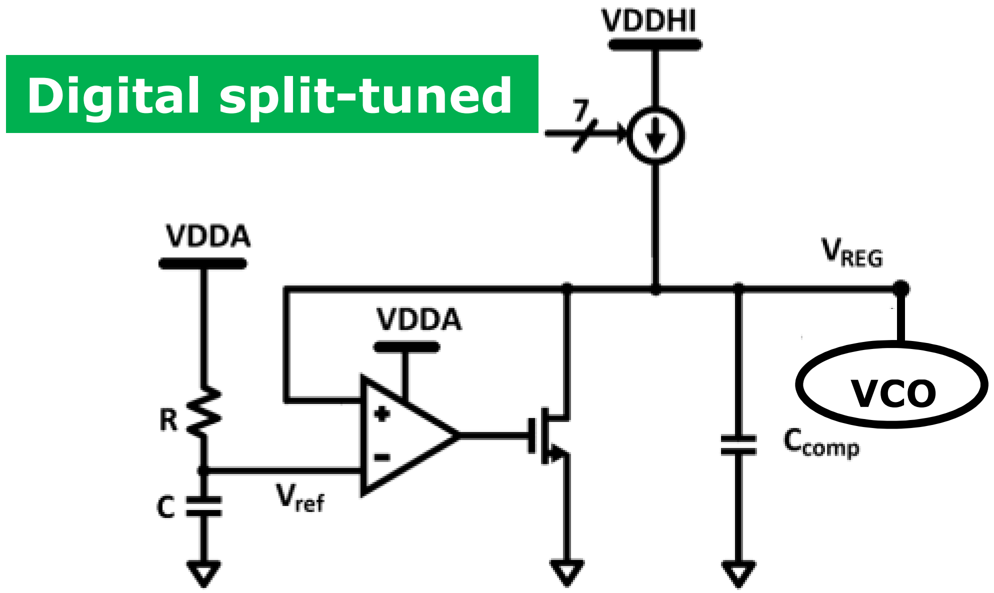


- 10-40dB power supply noise rejection ratio (PSRR)
- Regulator degrades power/current efficiency
- Bandwidth vs. power/area tradeoff
  - To avoid peaking in PSRR: Amplifier pole (ω_a) > regulator output pole (ω_o)
  - If inside the PLL/DLL loop, the regulator BW should be higher than loop BW

Examples of Regulator Topologies



E. Alon et al.,"Replica Compensated Linear Regulators for Supply-Regulated Phase-Locked Loops", JSSC 2006



T. Musah, et al., "A 4–32 Gb/s Bidirectional Link With 3-Tap FFE/ 6-Tap DFE and Collaborative CDR in 22 nm CMOS," JSSC 2014

- Improving PSRR response with minimum power and area penalty
  - Using "replica" or "split-tuned" to push amplifier pole to higher frequency
- Faster response time
  - Fast wakeup and clock power management

Outline

- Clock quality terminology
- Clocking architectures and circuits
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  - Clock distribution
  - Clock recovery
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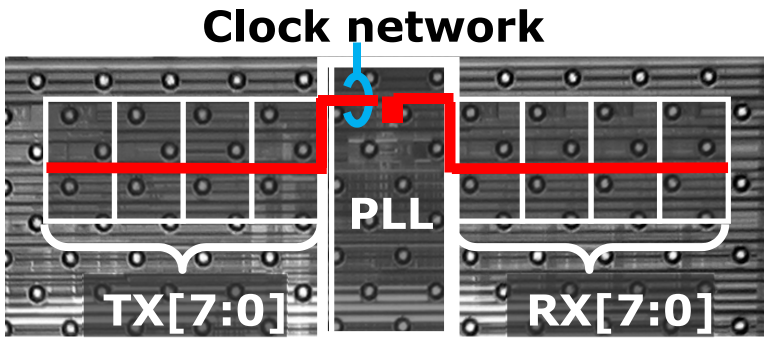
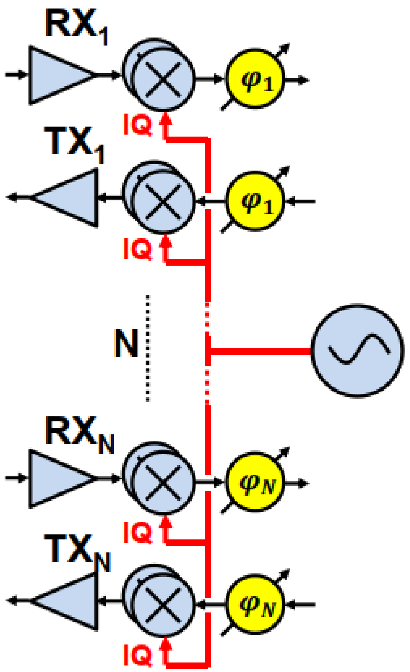
Clock Distribution Design Considerations

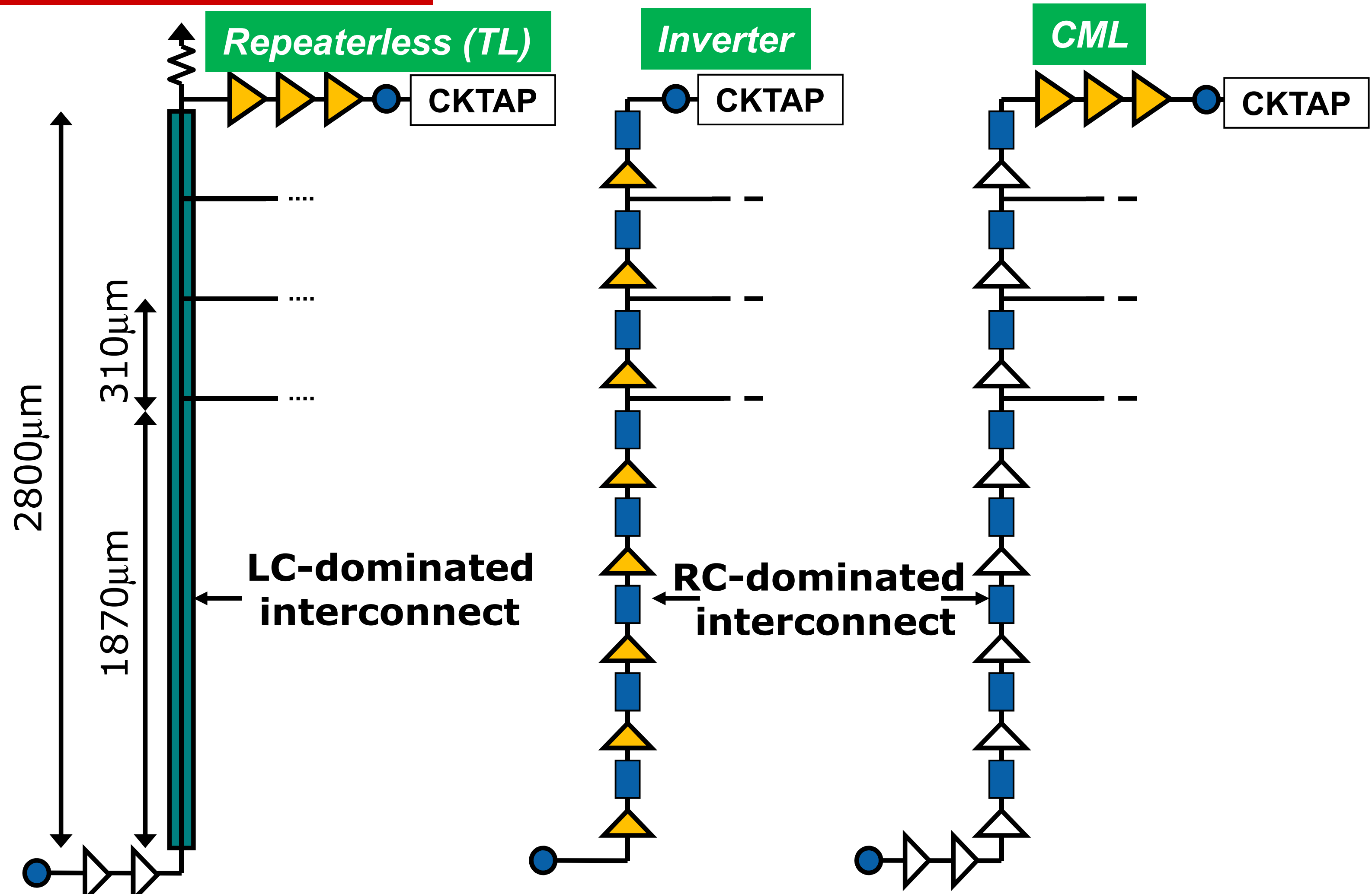
- Distribution from clock synthesizer to TX and RX lanes
  - Jitter/phase noise
  - Bandwidth/slew rate
  - Operating frequency range
  - Distribution vs. local clock frequency
  - Power (dynamic vs. static)
  - Area
  - Latency
  - Mismatch between IQ phases





Wireline Clock Distribution Example

- Clock distribution common topologies
  - Repeaterless (on-die transmission lines)
  - CMOS inverter buffers
  - CML buffers



F. O'Mahony et al, "A low-jitter PLL and repeaterless clock distribution network for a 20Gb/s link," VLSI 2006

Comparison Summary (10GHz)

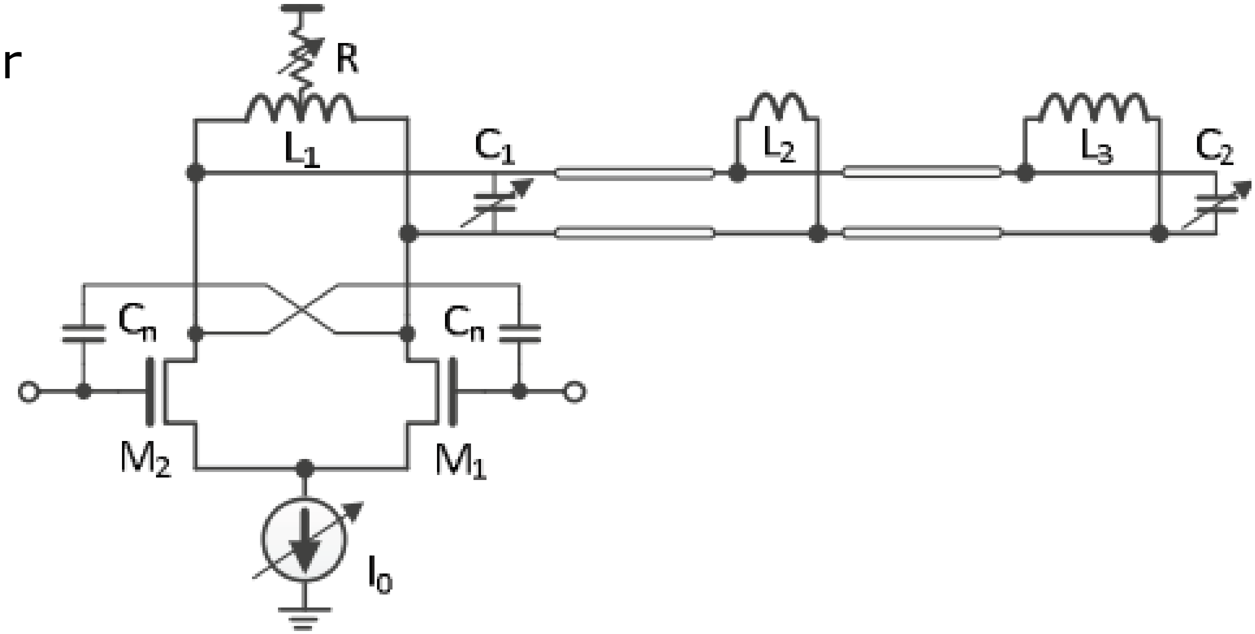
	Jitter [±ps] with ±5% Vcc noise	Latency [ps]	Power [mW]
Repeaterless (TL)	**1.0**	79	73
Inverter	3.2	96	**53***
CML	1.4	142	110

*** Zero static power**

- Repeaterless
  - 3.2x (10dB) better PSRR with 38% more power compared with inverter
  - 1.4x (3dB) better PSRR with 34% less power compared with CML
  - Area hungry and integration un-friendly
- Inverters are power and area efficient at cost of poor PSRR
  - Easy power management due to zero static current
  - Regulated supply: jitter vs. power/area/wakeup time

Repeaterless TL Topologies

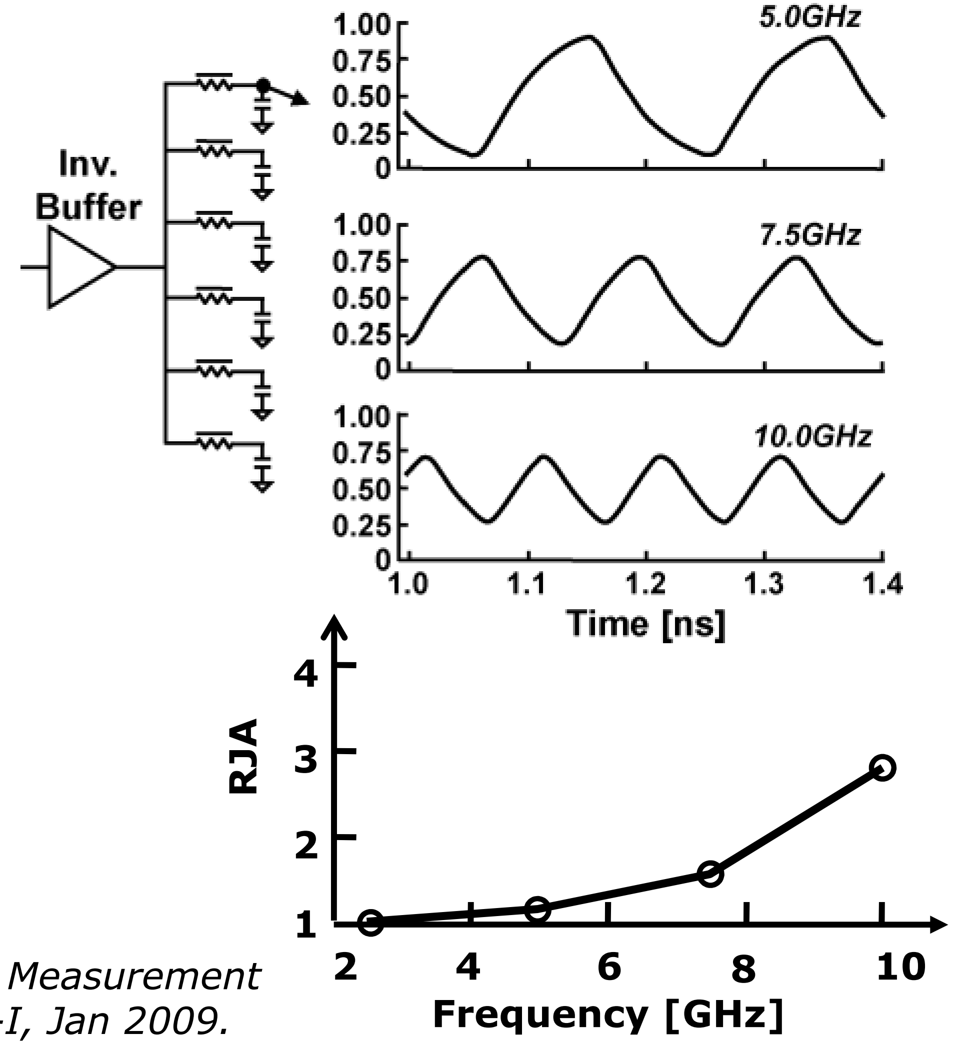
- Open-drain buffer w/ termination at output
  - ☑ Amplitude matched
  - ☒ Phase mismatched
  - ☒ Low-swing clock → needs level converter
- Standing wave based
  - ☑ 3-5x power reduction
  - ☑ Near full-swing clock
  - ☑ Phase matched
  - ☑ Minimized amplitude mismatch
  - ☒ Narrowband frequency
  - ☒ Routing< fraction of clock wavelength



G. Li et al, "Standing Wave Based Clock Distribution Technique with Application to a 10 × 11 Gbps Transceiver in 28 nm CMOS," *IEEE Asian Solid-State Circuits Conference 2015*

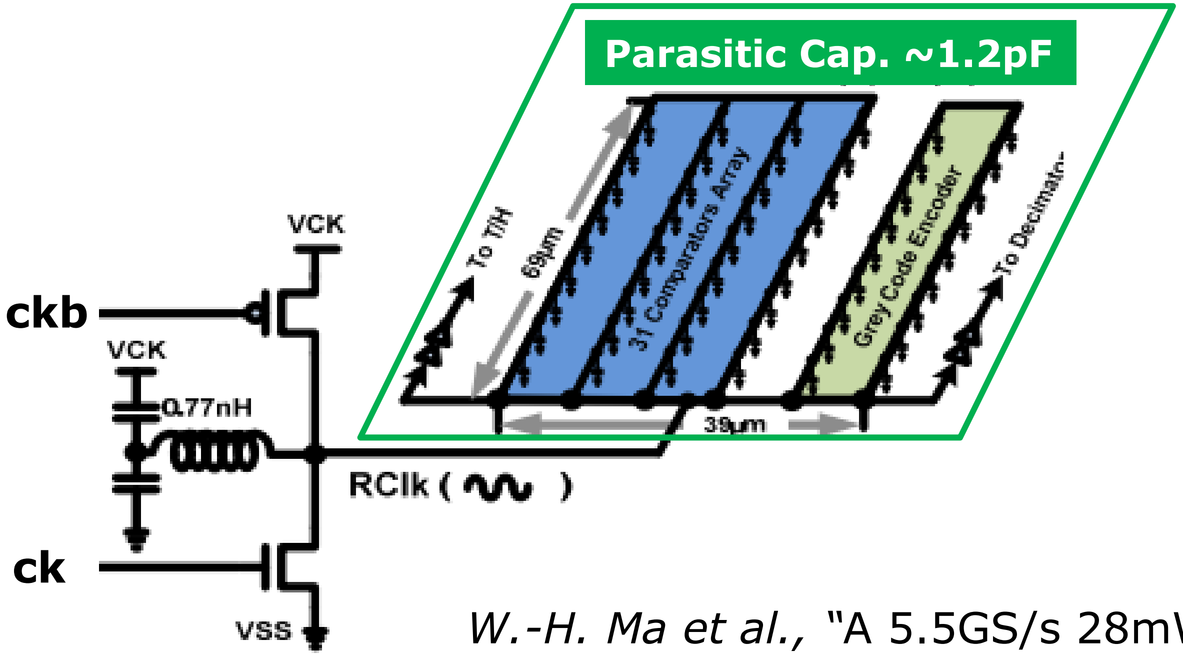
Clock Distribution Jitter Optimization

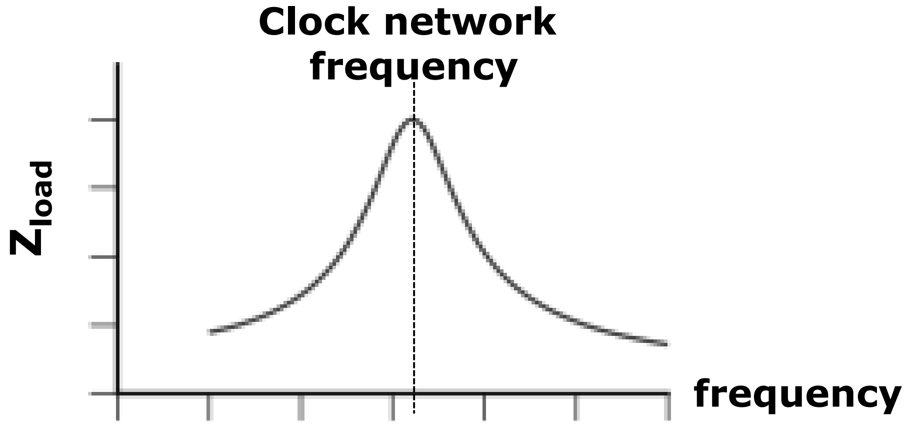
- Clock distribution can limit jitter/phase noise performance
  - Jitter generation
  - Input random jitter amplification (RJA)
- Power vs. jitter amplification
  - Ex: Inverter chain with lower fan-out (FO) minimizes RJA at cost of power
- Improving jitter and power
  - Self-oscillating clock networks or tuned LC to resonate with line capacitance



B. Casper et al., "Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links-A Tutorial," TCAS-I, Jan 2009.

Resonant Clock Network Example

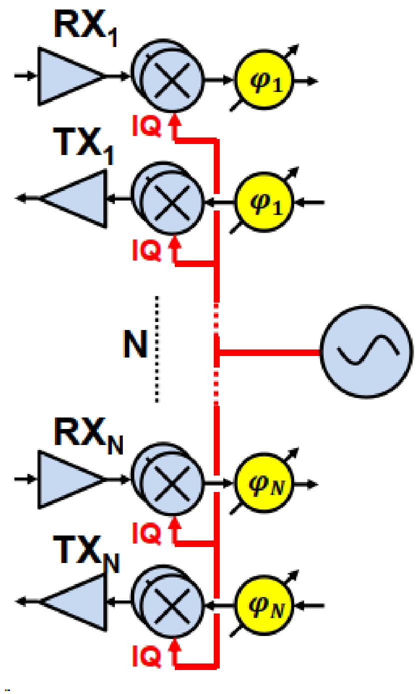




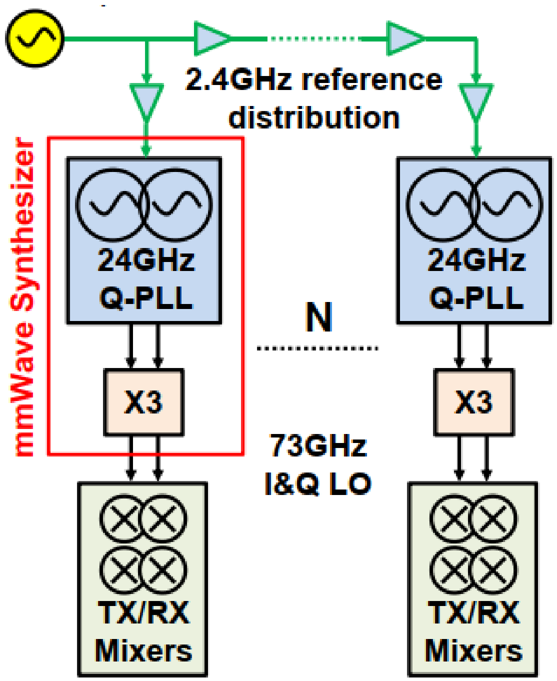
W.-H. Ma et al., "A 5.5GS/s 28mW 5-bit Flash ADC with Resonant Clock Distribution ," *ESSCIRC 2011.*

- Resonant clock distribution to drive a flash ADC
- 50% lower power compared to conventional inverter buffers (CV^2f)

Wireless LO Distribution Example



S. Pellerano et al., "A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver …", ISSCC 2019



- ☐ mmWave LO distribution
  - ☒ Many gain stages
  - ☒ I & Q mismatches
  - ☒ Lossy match to 50ohm TLs
- ☐ Low frequency reference distribution
  - ☑ Minimize distribution power
  - ☐ Local mmWave synthesizer
  - ☑ Better noise/power trade off

Clock Distribution Summary

- Circuit architecture and techniques to minimize
  - Jitter
  - Power
  - Area
- Repeaterless is an alternative to CMOS/CML distribution
- Resonant clock network achieves better BW/jitter and power performance
- Sub-harmonic LO distribution for better noise, power and IQ matching

Outline

- Clock quality terminology
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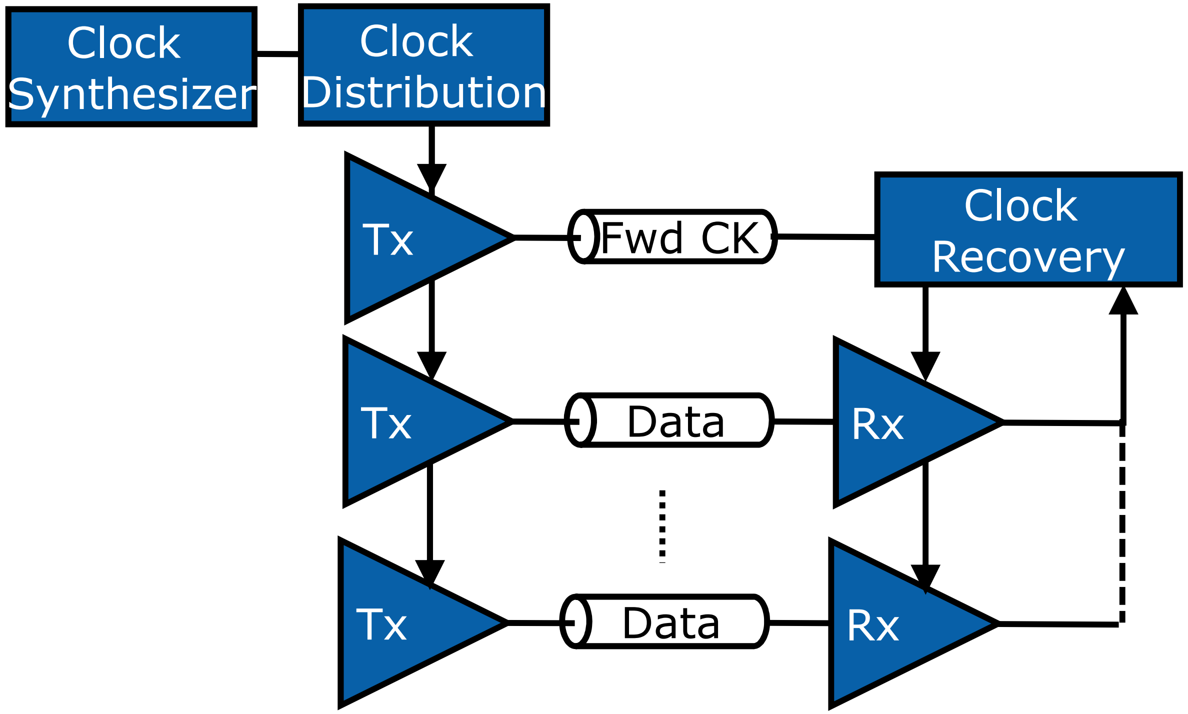
  - VCO
  - Clock distribution
  - Clock recovery
- Clock calibration
- Clock amortization and power management

Clock Recovery

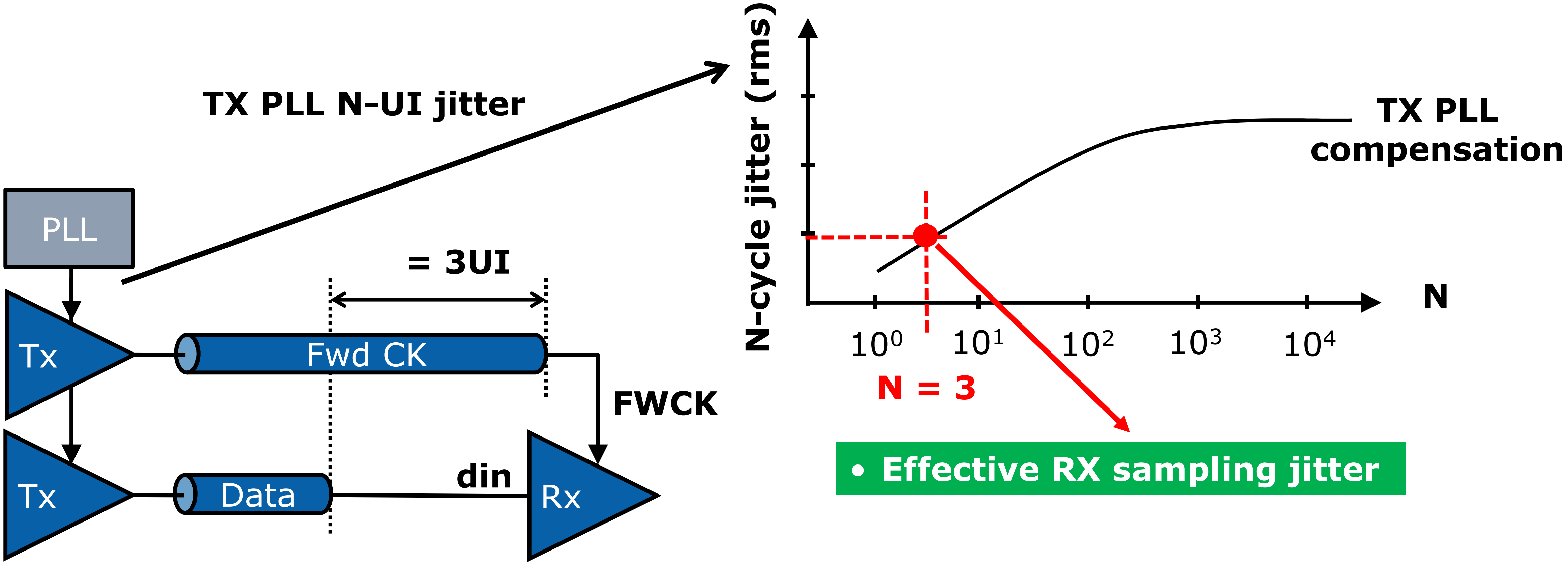
- Forwarded clock (FC) systems
- Embedded clock (EC) systems

Forwarded Clock (FC) Recovery



- Wide parallel link interfaces where Fwd CK overhead is amortized
  - Examples: DDRx, LPDDRx
- Recovery method
  - Extract timing from FC using training or periodic deskew

Differential Jitter in FC System

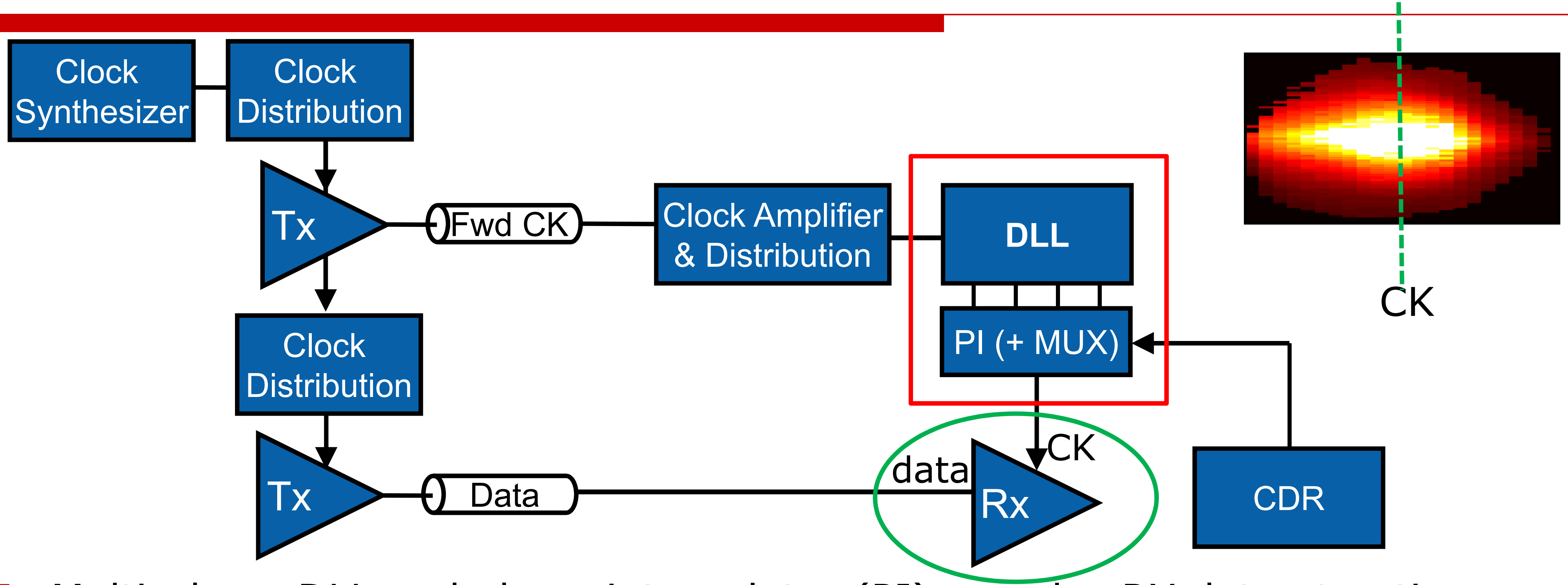


- Example shown for 3UI delay mismatch between Fwd CK and data path
  - Effective RX sampling jitter = Differential jitter between “FWCK” and “din”

FC Recovery Design Considerations

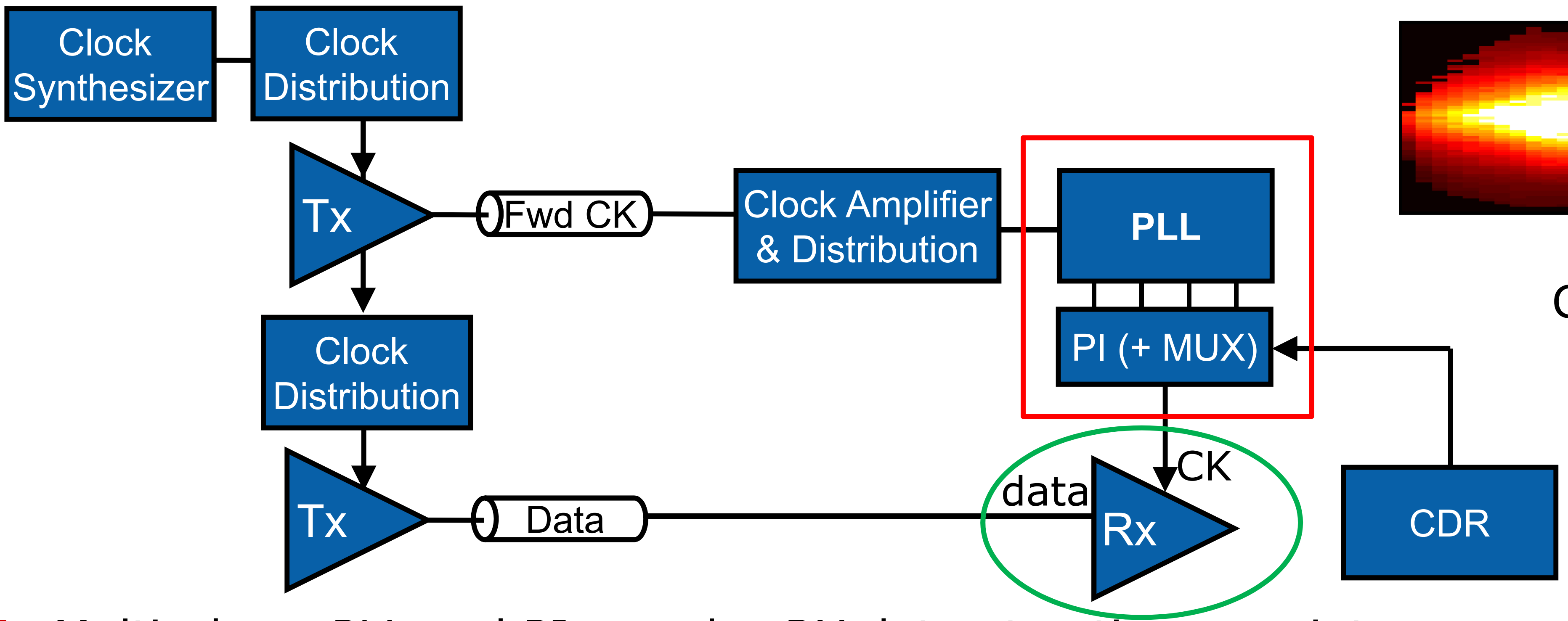
- Data-FC tracking is a key advantage
  - Jitter accumulation up to delay difference between two paths
  - Minimize delay mismatch between two paths
- Fwd CK jitter amplification due to channel loss
  - No filtering for DLL-based clock recovery (CR)
  - Filtering high frequency jitter using PLL or ILO-based CR
- Clock recovery
  - Low-bandwidth loop to compensate for voltage/temperature drift
  - Fine phase tuning of Fwd CK for optimum RX data sampling
  - DLL/PI vs. VCO/ILO-based forwarded clock

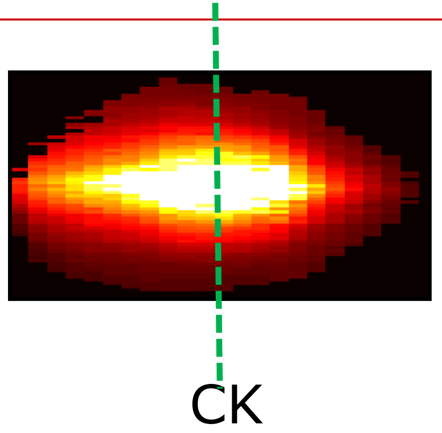
DLL-Based FC Recovery



- Multi-phase DLL and phase interpolator (PI) samples RX data at optimum point
  - ☑ Low-BW clock and data recovery (CDR) which sets PI code
  - ☑ No additional jitter accumulation (owing to DLL)
  - ☒ No filtering on Fwd CK

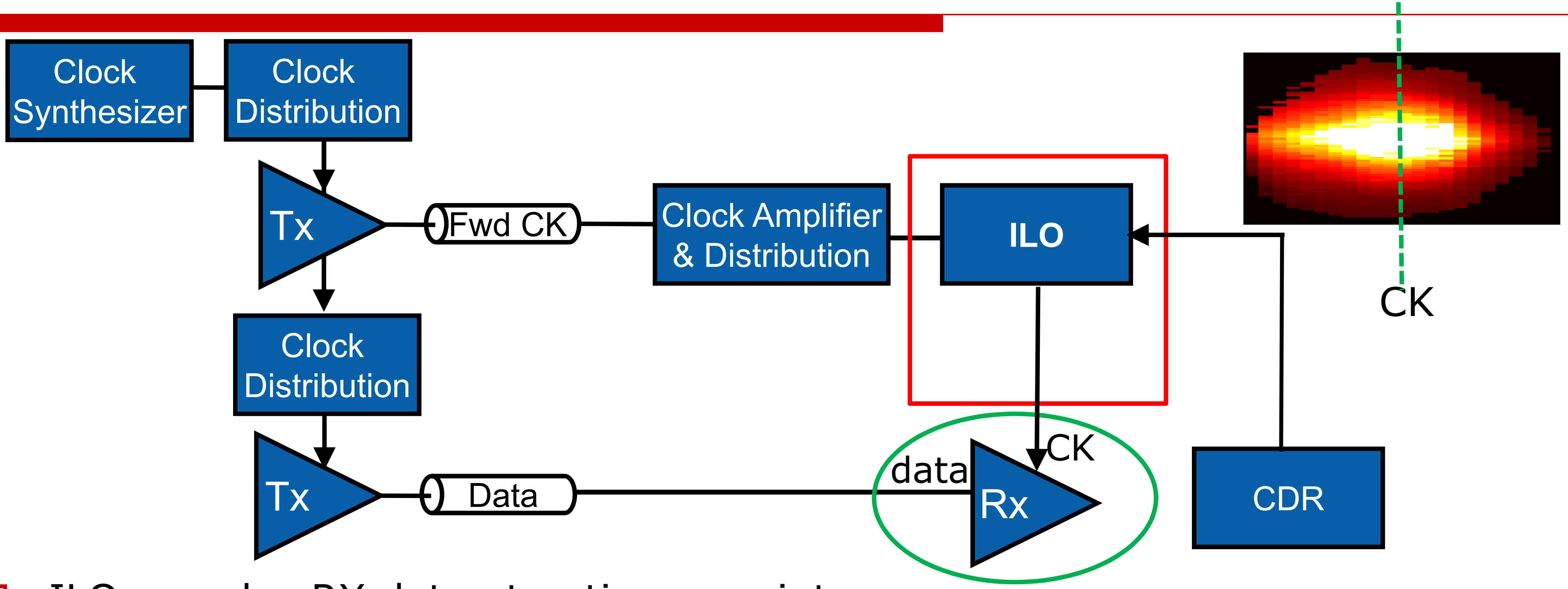
PLL-Based FC Recovery





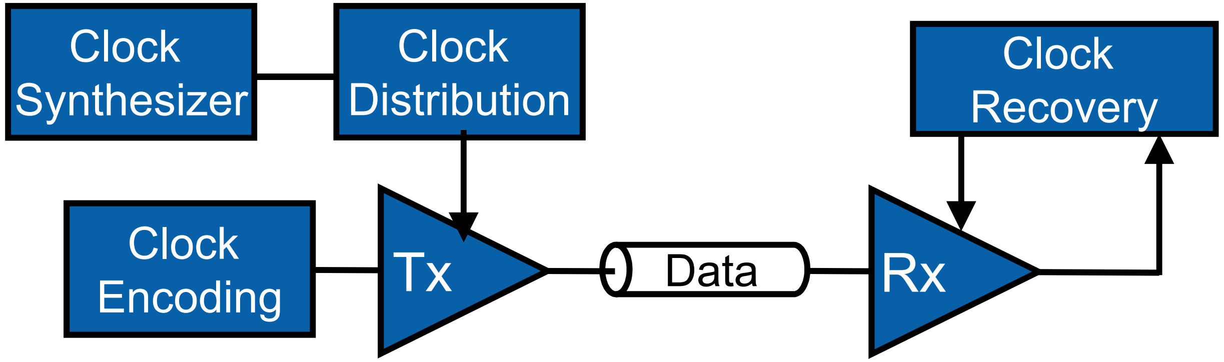
- Multi-phase PLL and PI samples RX data at optimum point
  - ☑ Low-BW CDR which sets PI code
  - ☑ Filters Fwd CK high frequency jitter
  - ☒ Reduces tracking BW between data and Fwd CK
  - ☒ Jitter accumulation

ILO-Based FC Recovery



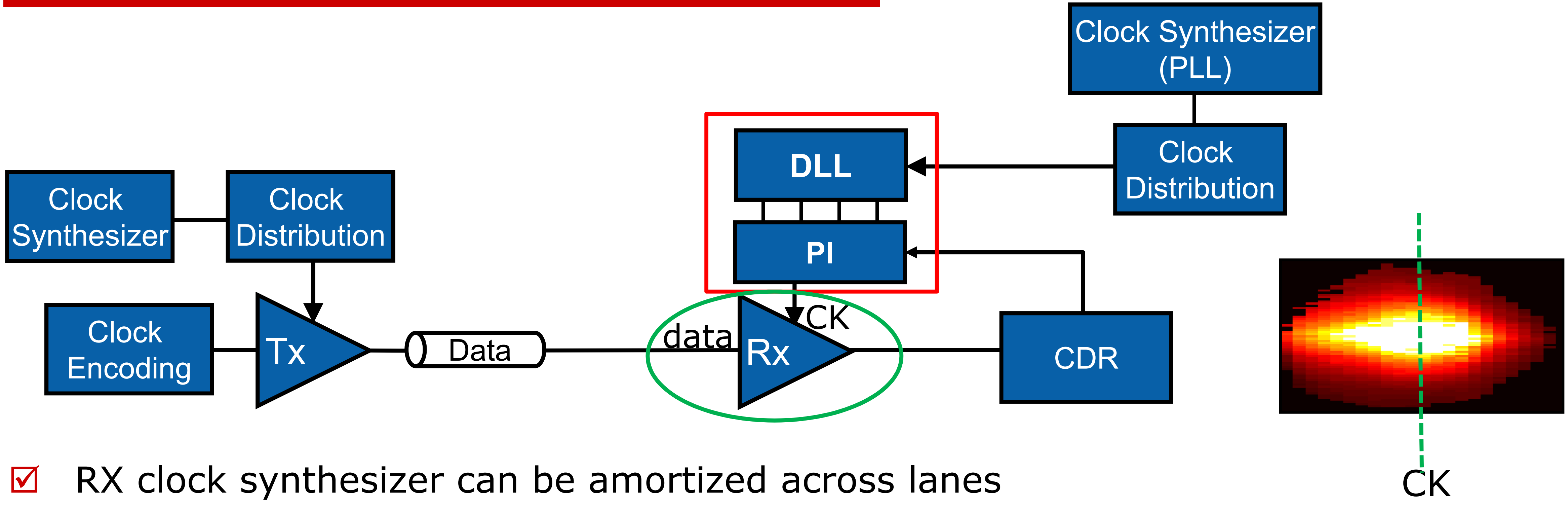
- ILO samples RX data at optimum point
  - ☑ Low-BW CDR which sets free-running frequency of VCO in ILO
  - ☑ Filters Fwd CK high frequency jitter (similar to PLL-based)
  - ☑ Higher tracking BW and less jitter accumulation than PLL-based

Embedded Clock (EC) Recovery



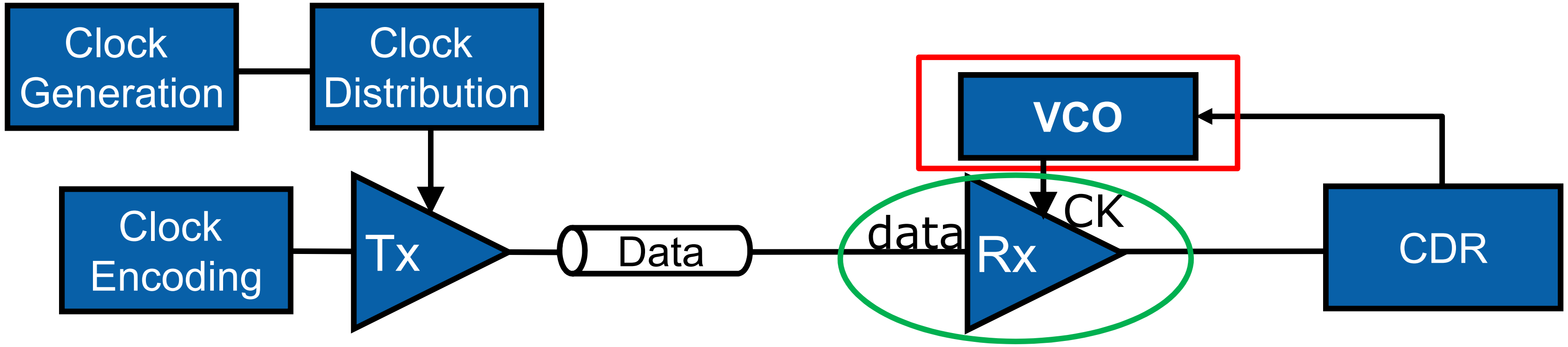
- SERDES interfaces
  - Examples: PCI-Express, USB
- Recovery method – Extract timing (phase & frequency) from data transitions
  - Timing info encoded (embedded) in data transitions → scrambling, 8b/10b, 64b/66b

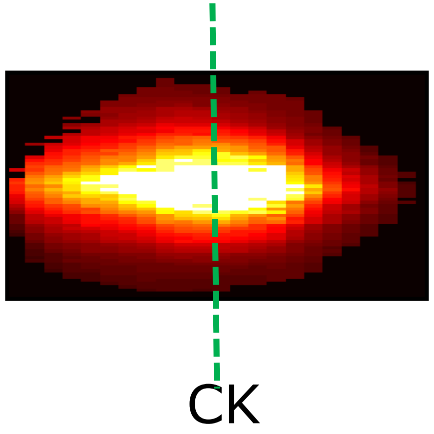
PI/Mixer-Based EC Recovery



- ☑ RX clock synthesizer can be amortized across lanes
  - ☒ Jitter accumulation and delay variation on RX clock path
- ☑ No Jitter accumulation in local CDR
- ☒ CDR must handle frequency difference between 2 clock domains
- ☒ Dynamic glitch in PI must be addressed

VCO-Based EC Recovery

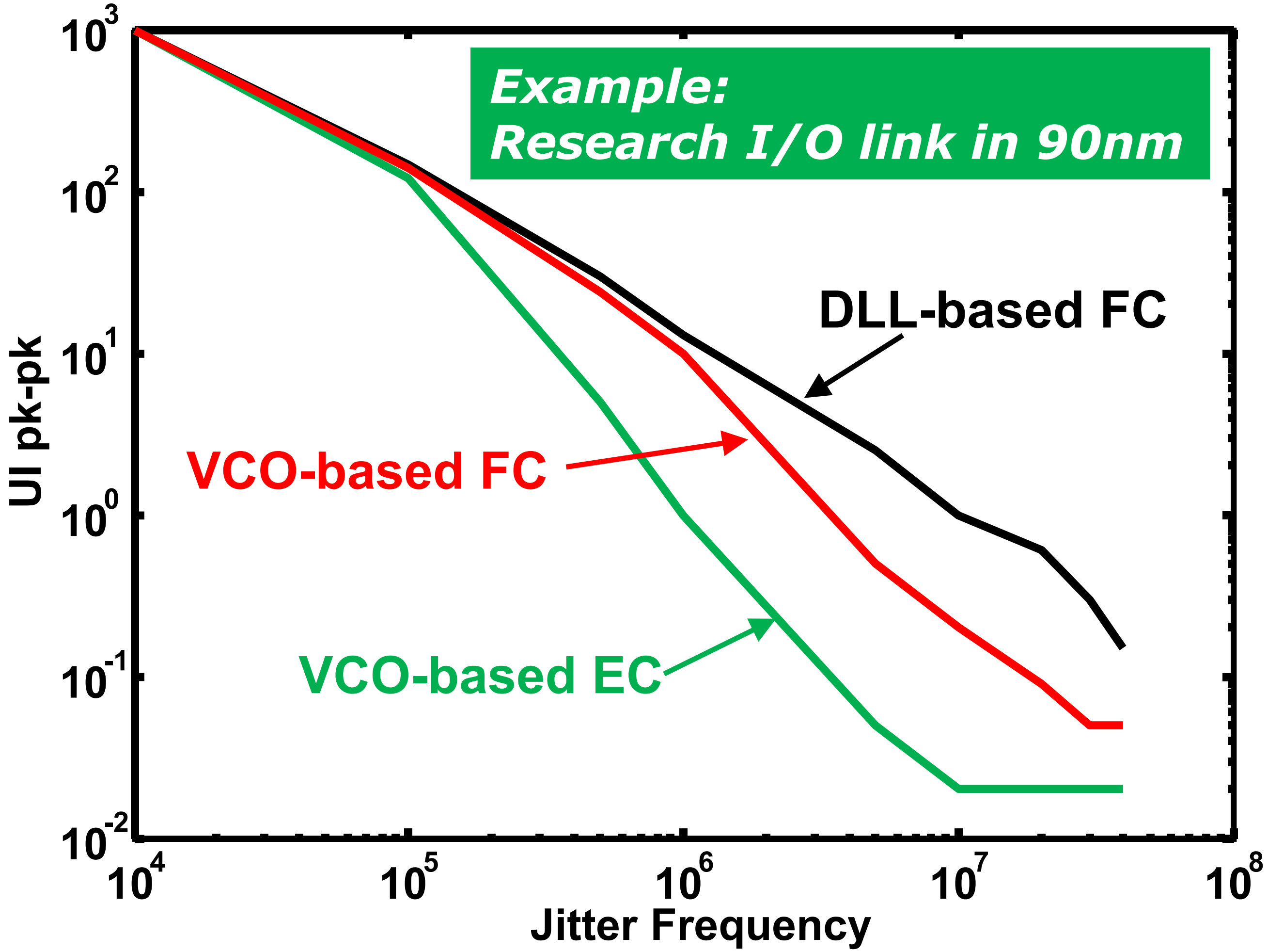




- ☑ One clock domain, within local RX
- ☒ VCO jitter accumulation
- ☒ Injection locking concern
- ☒ Larger area compared to PI-based

Jitter Tolerance Comparison

- DLL-based FC achieves best tolerance to input jitter (especially at higher frequency)
- VCO-based EC shows the worst tolerance to input jitter



Clock Recovery Summary

- Clock recovery architecture is often defined by standard/specification

- FC achieves better jitter and power performance, at cost of an additional clock channel

- Different architecture considerations for FC and EC
  - Tracking bandwidth and jitter performance
  - Power and area tradeoffs

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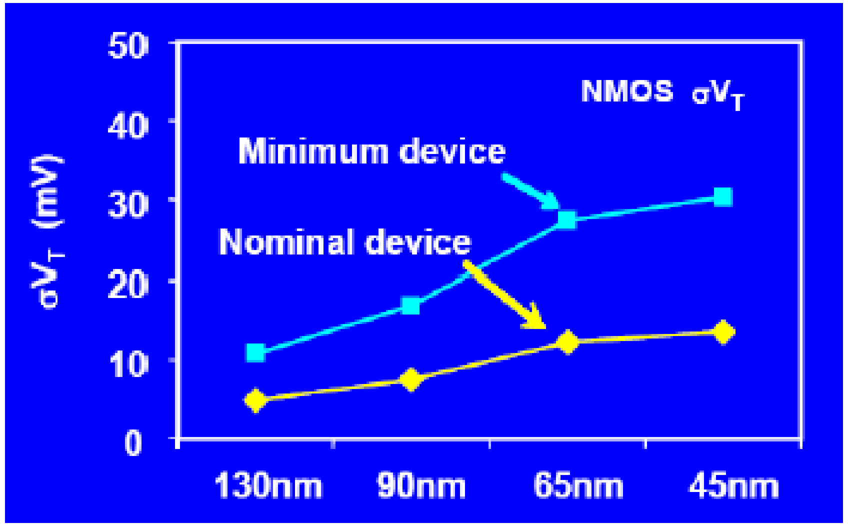
Process Scaling

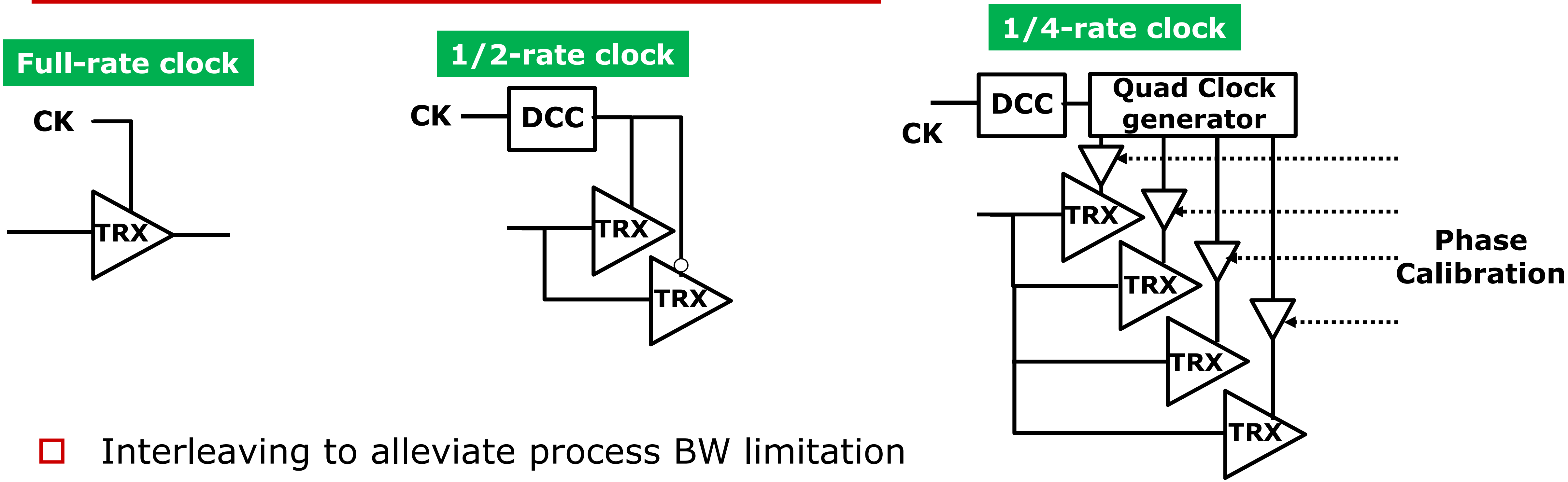
- Data rate scaling enabled in part by process scaling
  - Past: optimized for performance/bandwidth
  - Present: optimized for power
- Process variation increases by scaling due to smaller device area
- Interleaving techniques to mitigate process limitation
  - Complex multi-phase clocking circuits
  - Variation-tolerant techniques such as duty-cycle & multi-phase correction



$$\sigma V_T = \frac{1}{\sqrt{2}}\left(\frac{c_2}{\sqrt{Weff \cdot Leff}}\right)$$

K. J. Kuhn, "Reducing variation in advanced logic technologies: Approaches to process and design for manufacturability of nanoscale CMOS," IEDM, Dec. 2007

Clocking in Interleaving Architecture



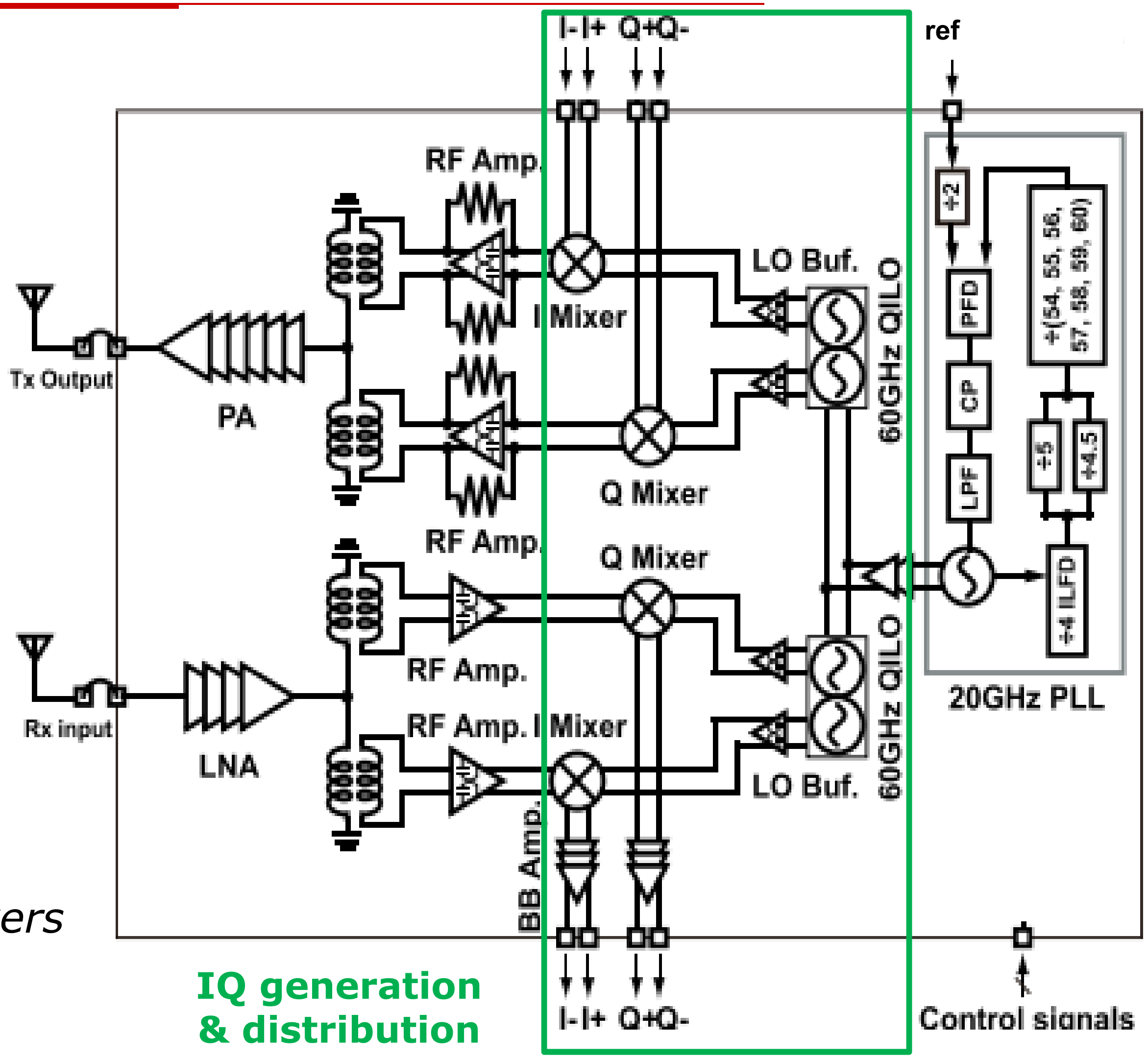
- Interleaving to alleviate process BW limitation
- Additional complexity of clock circuit design & calibration
  - Duty-cycle correction
  - Multi-phase clock generator (such as quadrature phases)

Clock calibration to detect/correct for process variation induced error

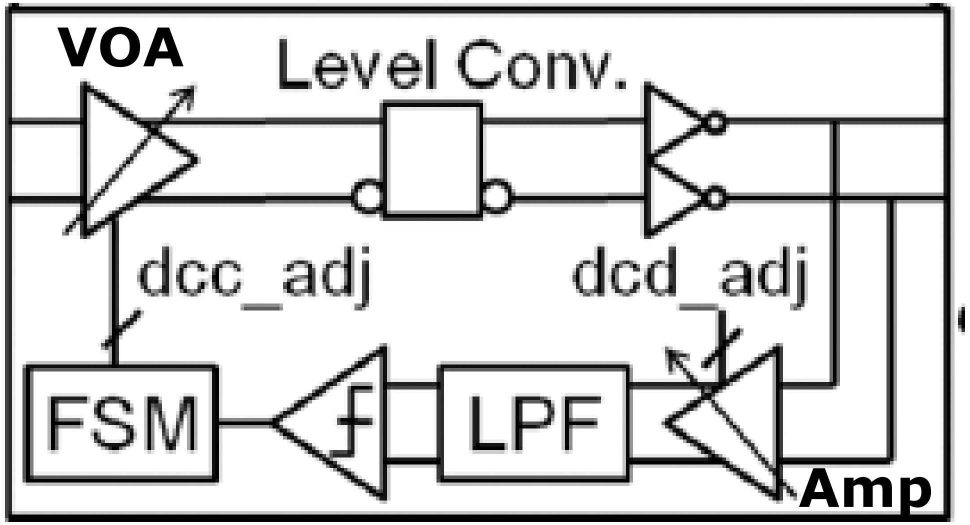
Quadrature Clocks in Wireless Applications

- Quadrature (IQ) clock phases at mm-wave
- Higher-order modulation (16/32/64-QAM)
- I & Q mismatches in mmwave
  - Constellation error
  - Calibration is required

R. Wu, et al., "64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay," JSSC, Nov. 2017

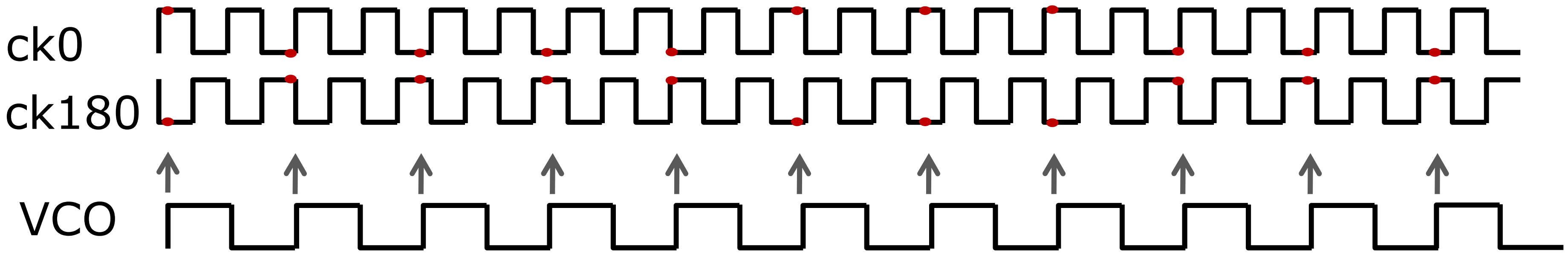


Conventional Duty-Cycle Detector (DCD)



- Clock is sampled by an amplifier & low-pass filtered to generate error
- Error code drives a variable offset amplifier (VOA) to correct for DCE
- Feedback Loop is mostly analog
  - Self-calibration of “Amplifier” to correct for induced offset
  - Large analog loop filter

All-Digital DCD

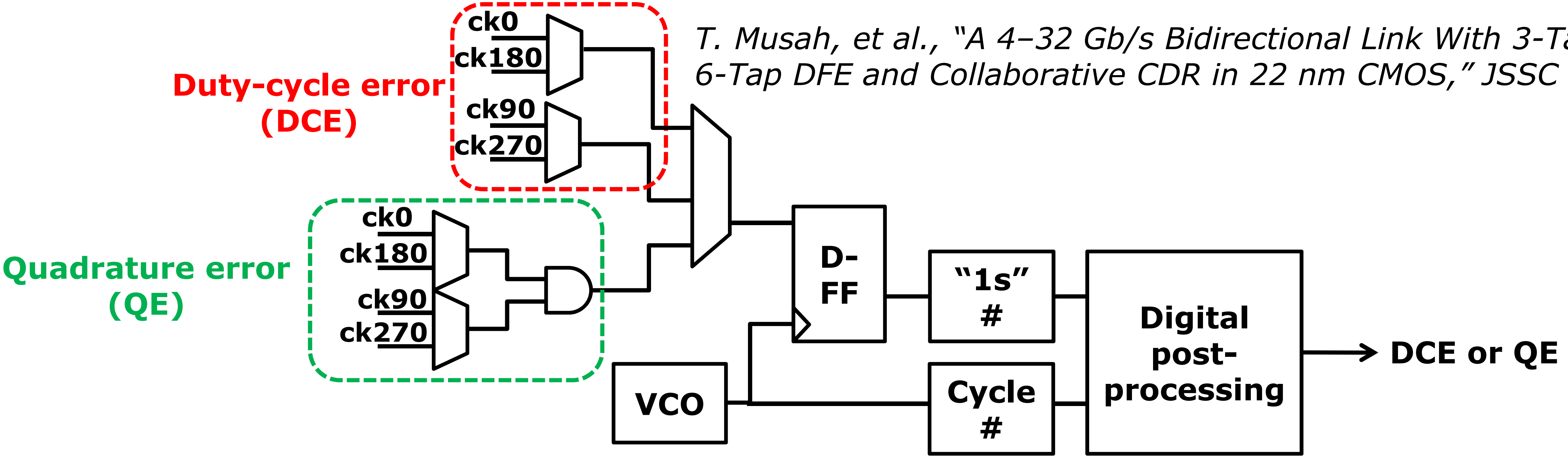


- VCO runs asynchronously with clock under test to generate uniform edge density
- Average-based technique
- Duty cycle error (DCE) is equal to probability* of “1s”
- Differential measurement limits effect of sampler non-idealities

DCE ∝ (Prob. of “1s” for ck0 - Prob. of “1s” for ck180)

* ratio of measured “1s” to total VCO cycles

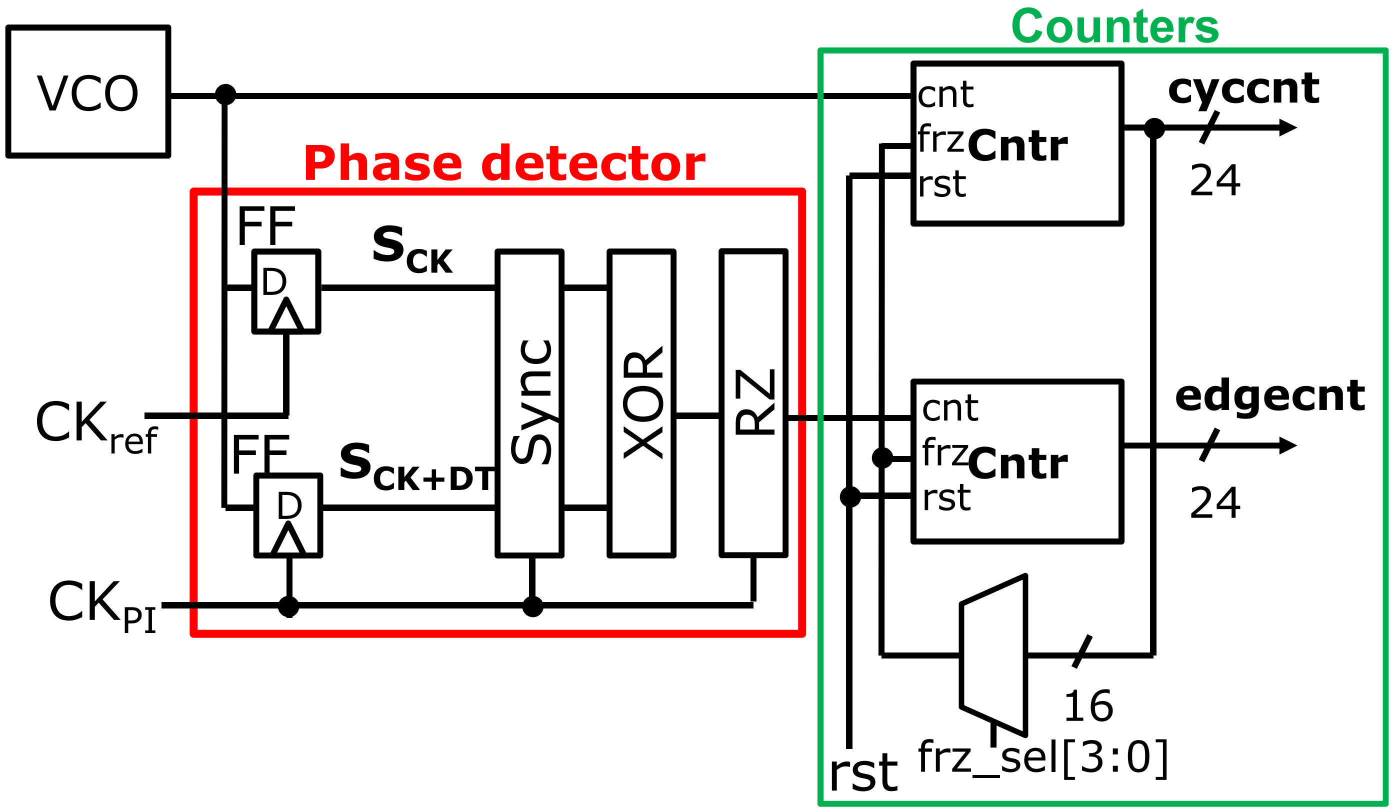
DCD & Quadrature Error Detector



T. Musah, et al., "A 4–32 Gb/s Bidirectional Link With 3-Tap FFE/ 6-Tap DFE and Collaborative CDR in 22 nm CMOS," JSSC 2014

- Fully digital implementation, including VCO
- Small area, mainly occupied by counters
  - Counter bits set measured accuracy
- DCC/QEC can be done during training and/or as background calibration

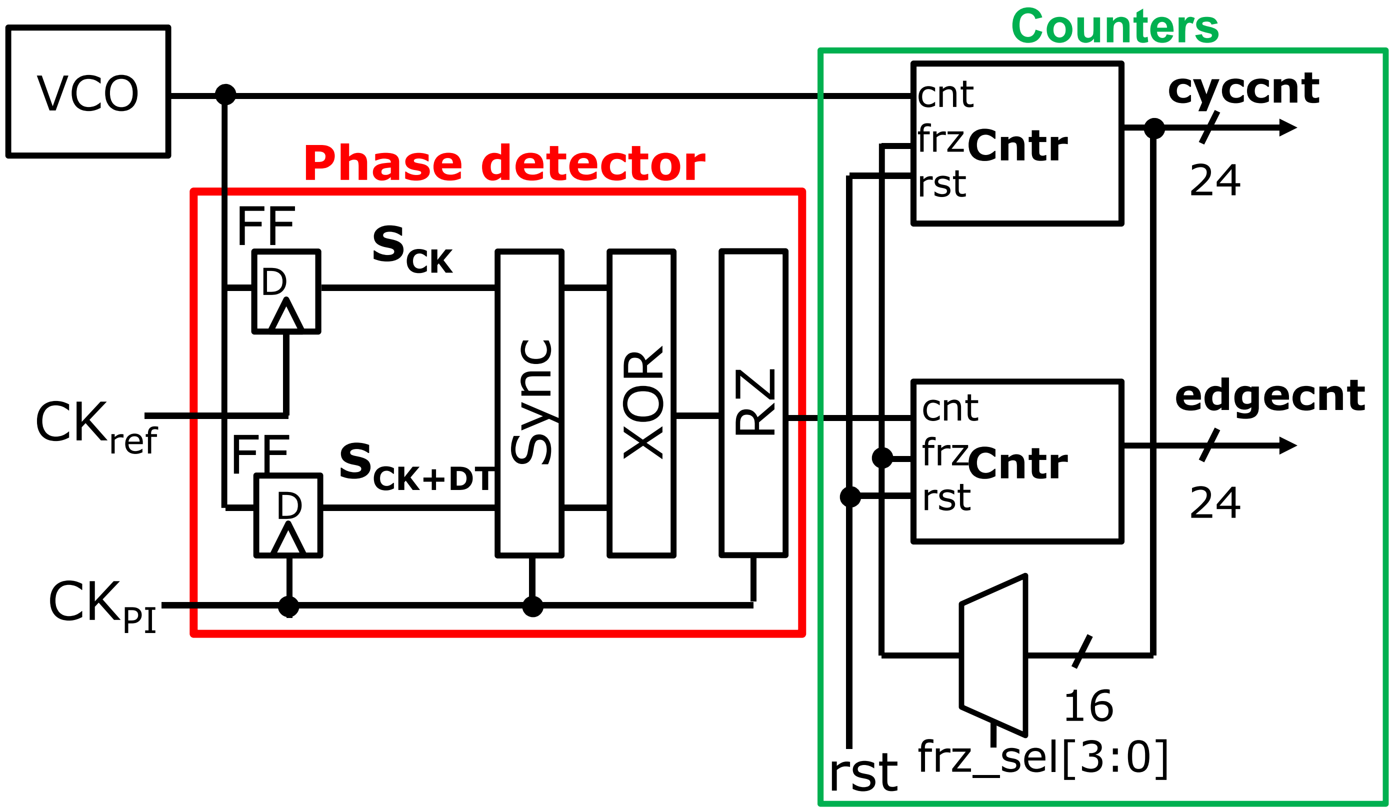
Delay Analyzer for PI Characterization



M. Mansuri, et al., "An On-Die All-Digital Delay Measurement Circuit with 250fs Accuracy," VLSI 2012

- PI characterization to calibrate and correct for INL and DNL
  - Phase detector + VCO and counters (similar to DCD/QED)

Delay Analyzer for PI Characterization



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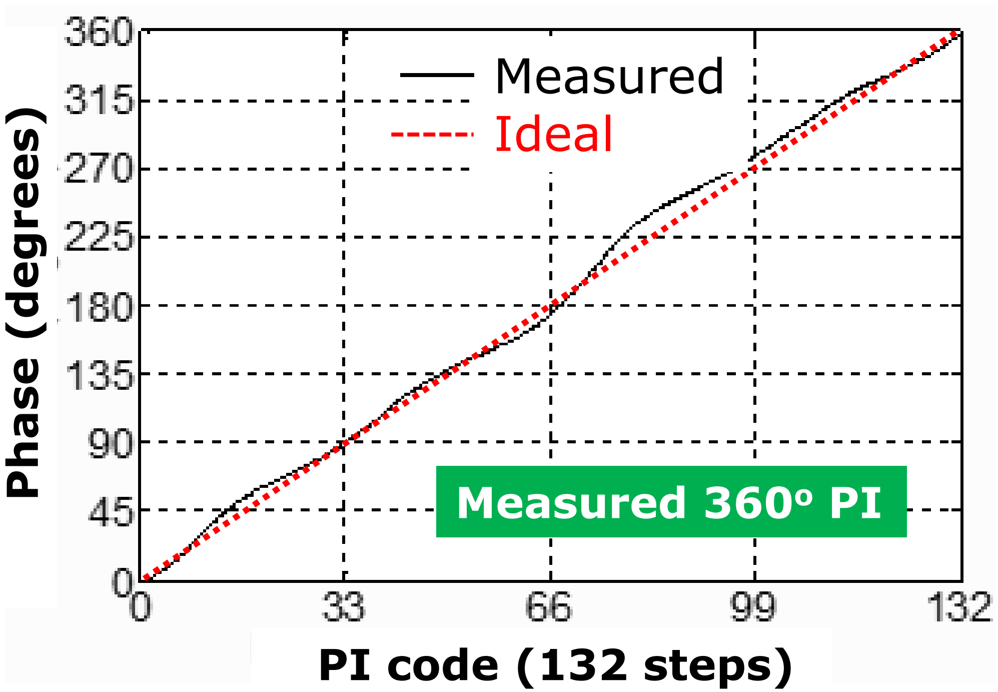


- PI characterization to calibrate and correct for INL and DNL
  - Phase detector + VCO and counters (similar to DCD/QED)

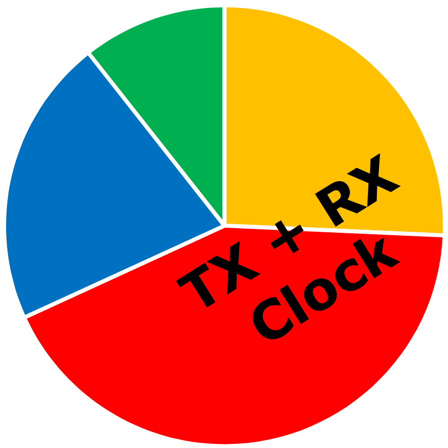
Clock Calibration Summary

- Clock calibration is a must to mitigate process variation
- In-situ measurement & correction
- Accuracy tradeoffs
  - Measurement time (average-based implementation)
  - Detector residual self-induced error
- Small area and low leakage
- All digital & scalable
  - No analog circuit or bias
  - Digital filter instead of RC filter

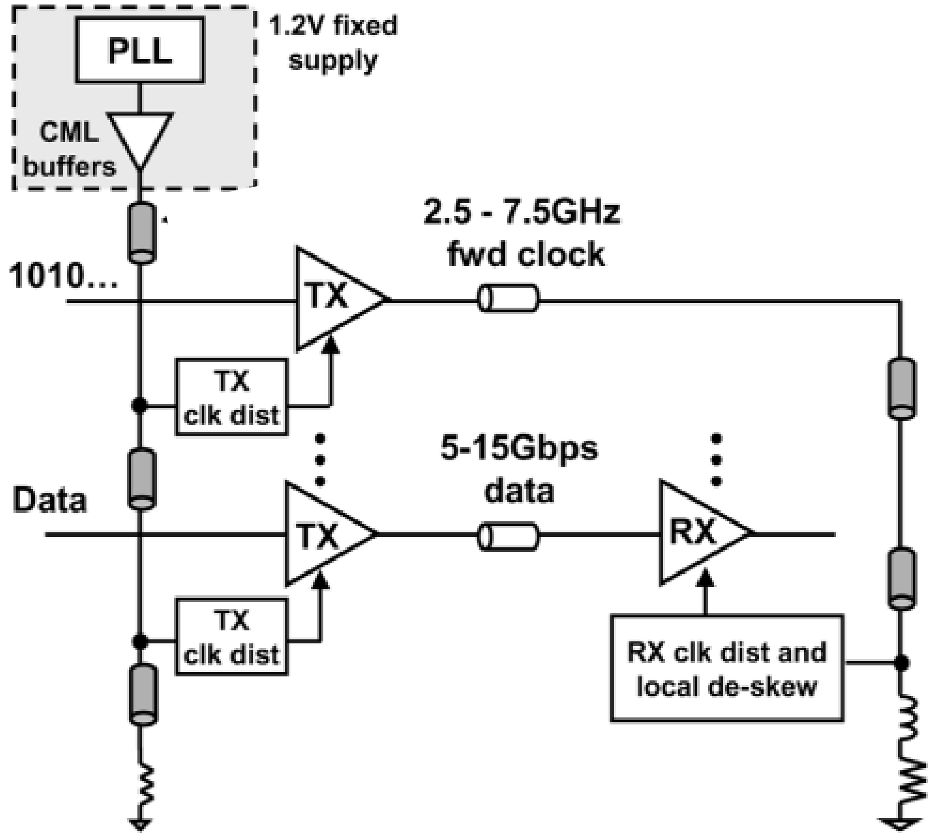
Outline

- Clock quality terminology
- Clocking architectures and circuits
  - Clock synthesizer
  - VCO
  - Clock distribution
  - Clock recovery
- Clock calibration
- Clock amortization and power management

Clocking Circuits Power

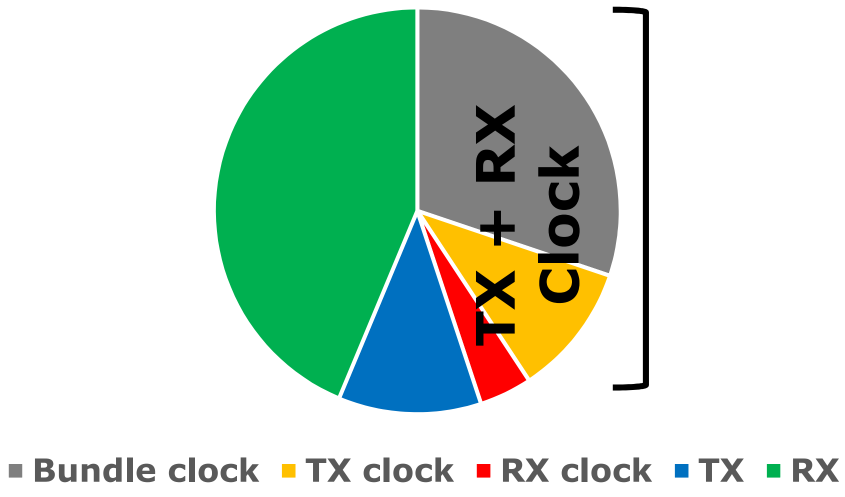


G. Balamurugan, et al., "A Scalable 5–15 Gbps, 14–75 mW Low-Power I/O Transceiver in 65 nm CMOS," *JSSC 2008*

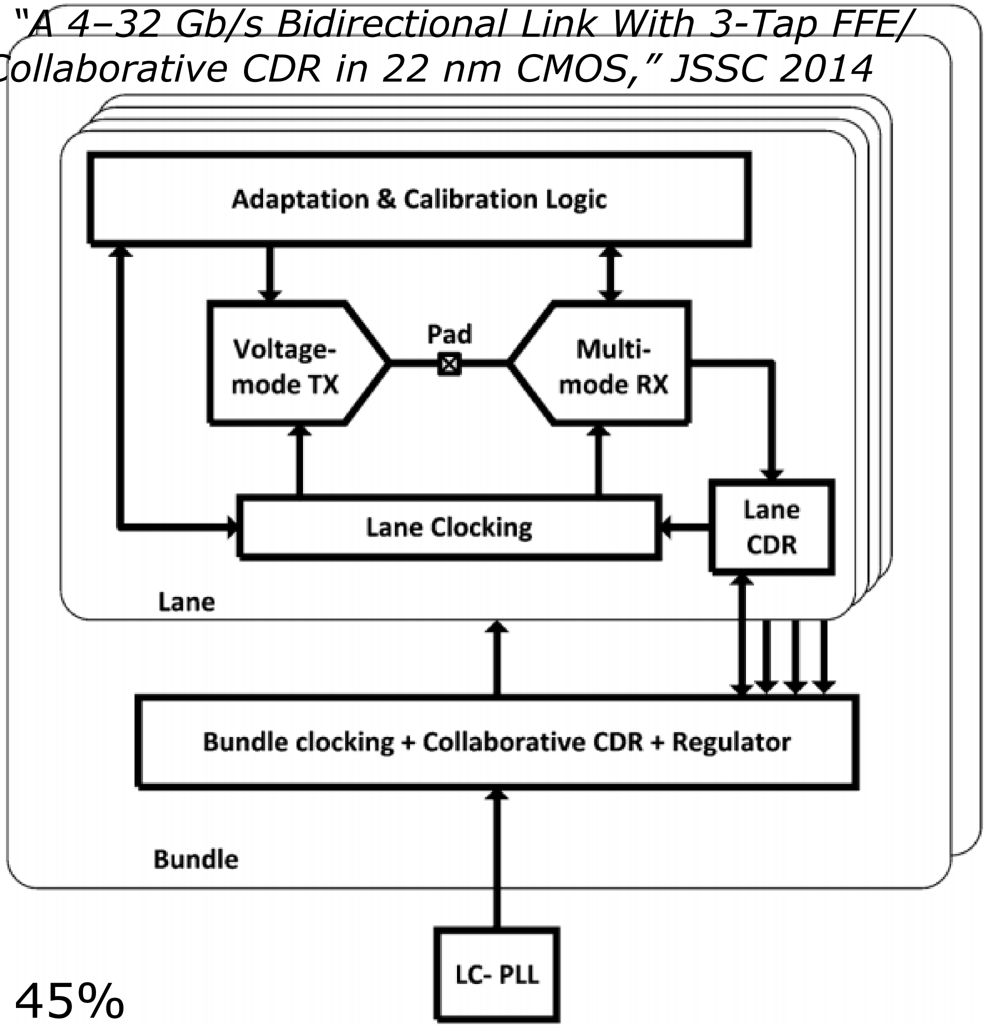


- Clocking circuits power is a good portion of system power
  - Example: clocking is 67% of total power
- Innovation in clocking circuits and amortization
- Power management

Clock Power Amortization



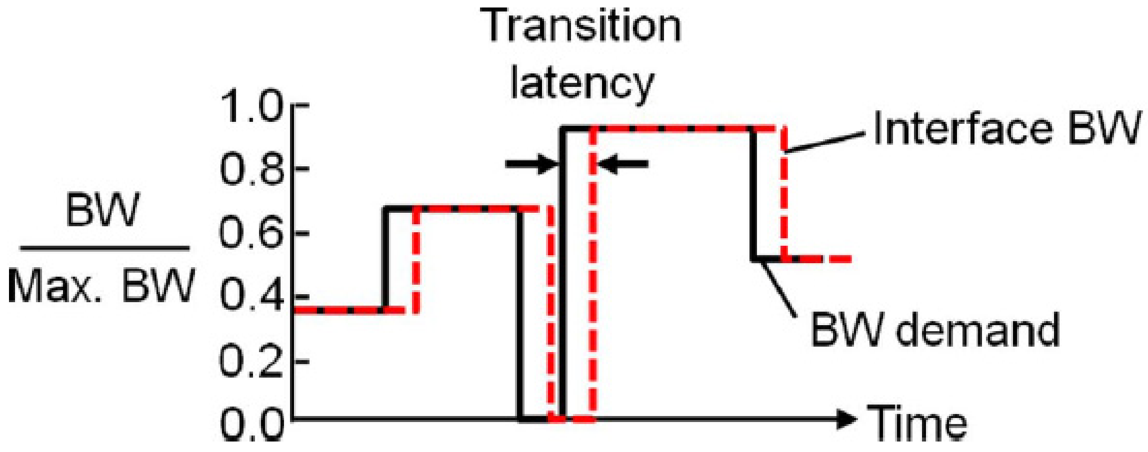
T. Musah, et al., "A 4–32 Gb/s Bidirectional Link With 3-Tap FFE/ 6-Tap DFE and Collaborative CDR in 22 nm CMOS," JSSC 2014



- Sharing clock to reduce clock power & area overhead
  - Bundle clock & collaborative CDR to share across lanes
  - Power-efficient clock distribution
  - Example: clocking power reduces from 67% to 45%

Clock Power Management

Hypothetical Link BW Demand



F. O'Mahony et al., "A 47x10Gb/s 1.4mW/(Gb/s) parallel interface in 45nm CMOS," JSCC, Dec. 2010

- Various power states: sleep, standby, active
- Minimum static power
- Frequency scaling as BW demand changes (to non-linearly save power)
- Fast frequency hopping and wakeup time (to reduce transition latency)
  - Challenges due to feedback loop latency (PLLs, DLLs, LDOs,…)

Clock Amortization and Power Management Summary

- Clocking power optimization to meet overall system power budget
- Global clock amortization among multi lanes and minimizing local clock power
- Power-efficient clock distribution
- Clocking design tradeoffs to enable fast wakeup time and frequency hopping for optimum power management

Summary

- Accurate clocking solutions are key enablers to aggressively scale data rate
- Clocking architecture/design tradeoffs, such as clock synthesis, recovery and distribution, for optimum jitter/phase noise and power performance
- Variation-tolerant clocking circuits to mitigate process scaling challenges
- Clocking circuit innovation and amortization to reduce power/area overhead
- Fast clock wakeup techniques with minimum standby power to enable aggressive power management

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