Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications

Boris Murmann
Stanford University
Stanford, CA, USA
murmann@stanford.edu

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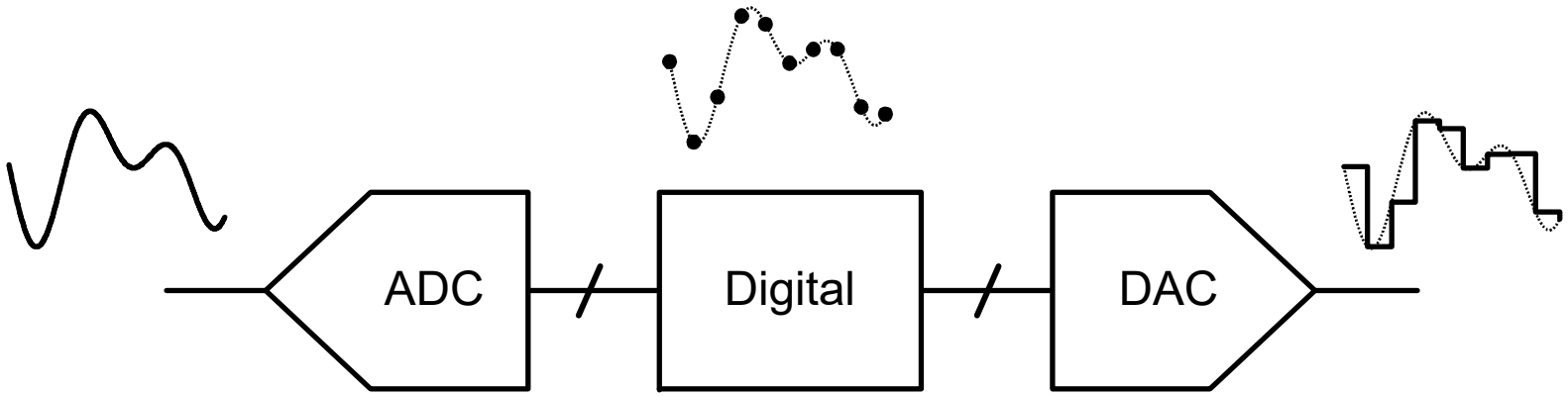
Self Introduction

- PhD from UC Berkeley in 2003
- Professor at Stanford University since 2004
- Interests
  - Sensor interfaces
  - Data converters
  - High-speed communication
  - Embedded machine learning

Boris Murmann

Objective

- Prepare attendees for subsequent deep-dive presentations
  - What are the relevant performance metrics?
  - What are the basic converter topologies?
  - What are the performance trends and limitations?
  - What are the application drivers and considerations?

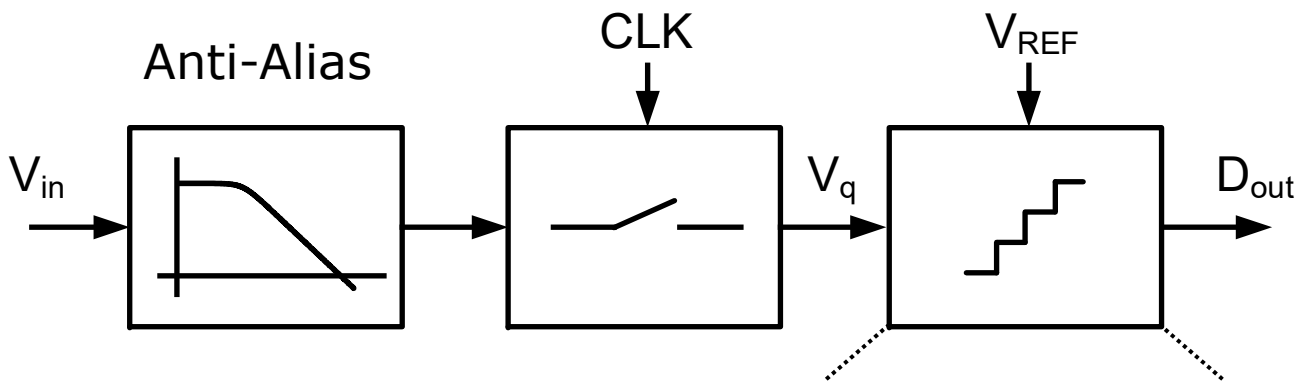


Outline

- ADCs
  - Metrics
  - Architectures
  - Speed, resolution, energy tradeoffs and trends
  - Building block considerations
  - Application aspects

- DACs
  - Output spectrum & metrics
  - Introduction to current steering
  - Timing and jitter requirements
  - Performance trends
  - Application aspects

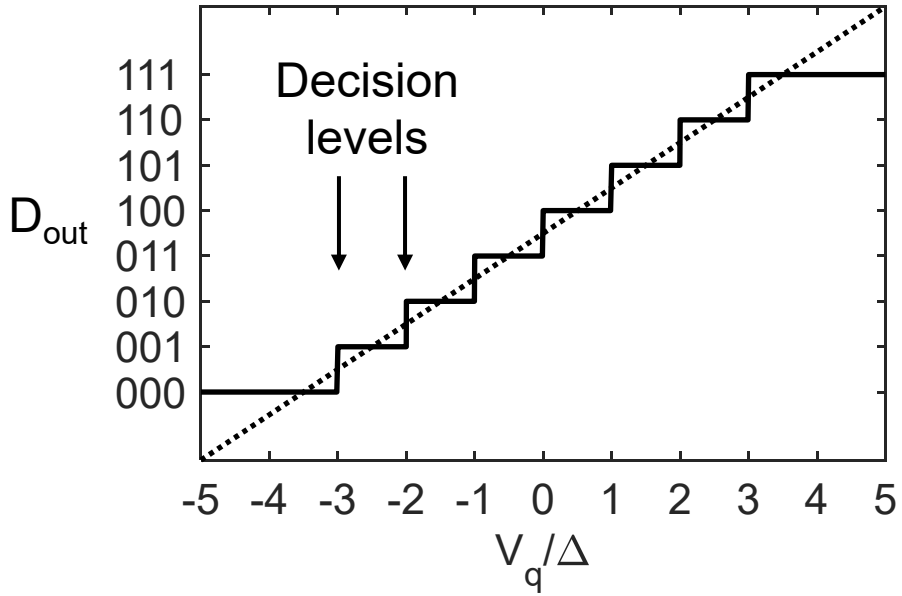
Generic A/D Interface

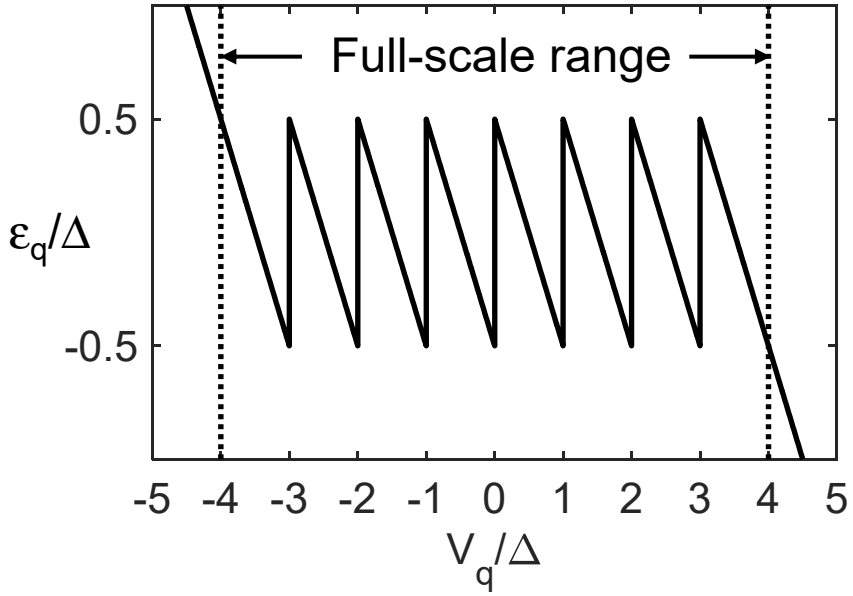


Δ = Step size (LSB size)
ε_q = Quantization error

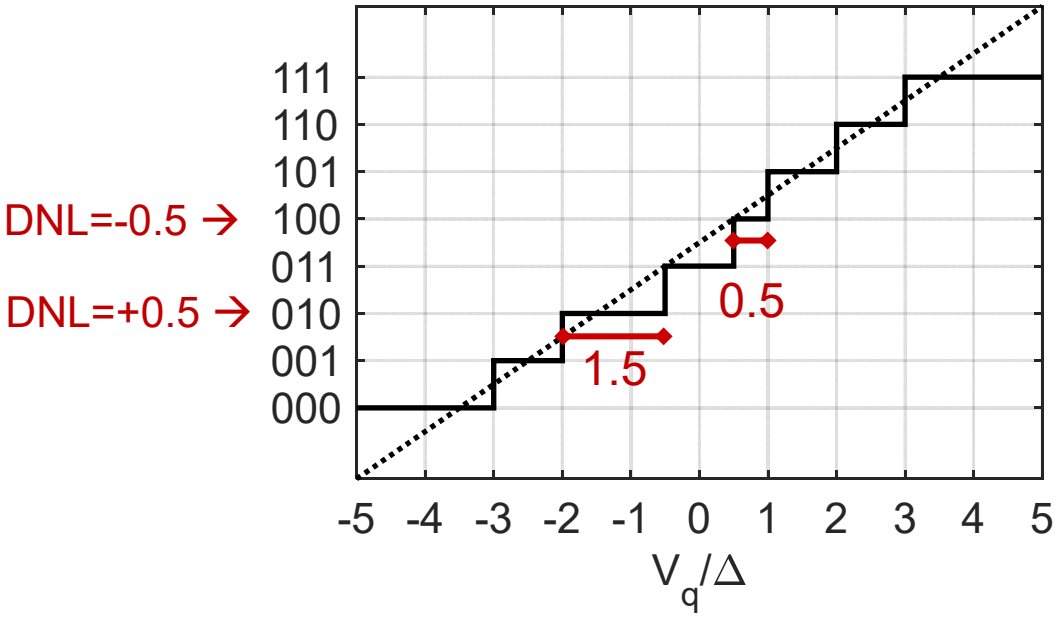
Signal-to-Quantization Noise Ratio for
B-bit quantizer and full-scale sinusoid

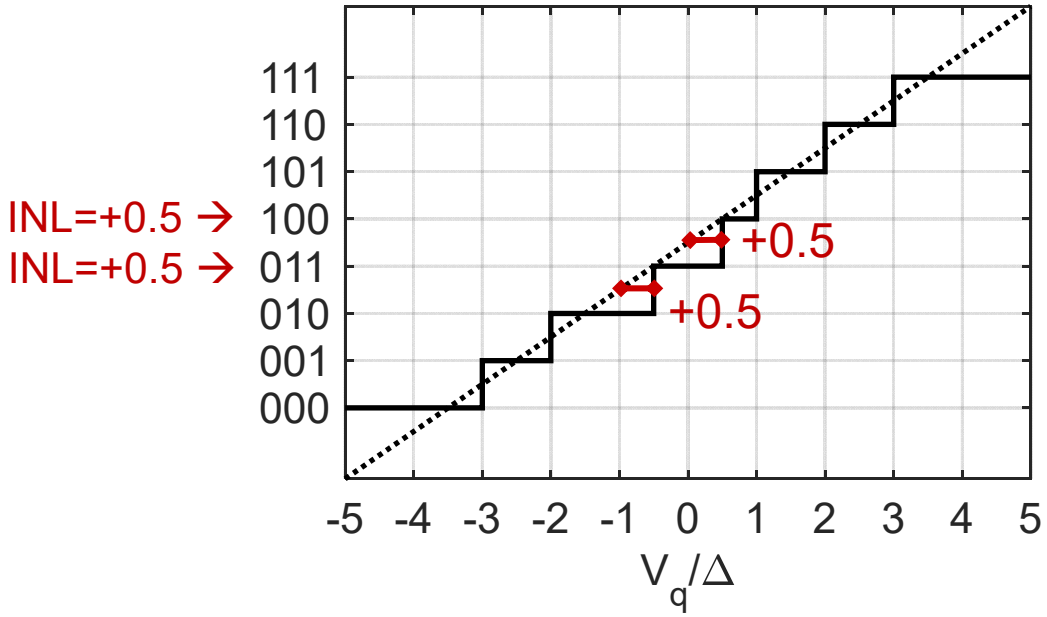
$$SQNR = 6.02 \times B + 1.76\ dB$$





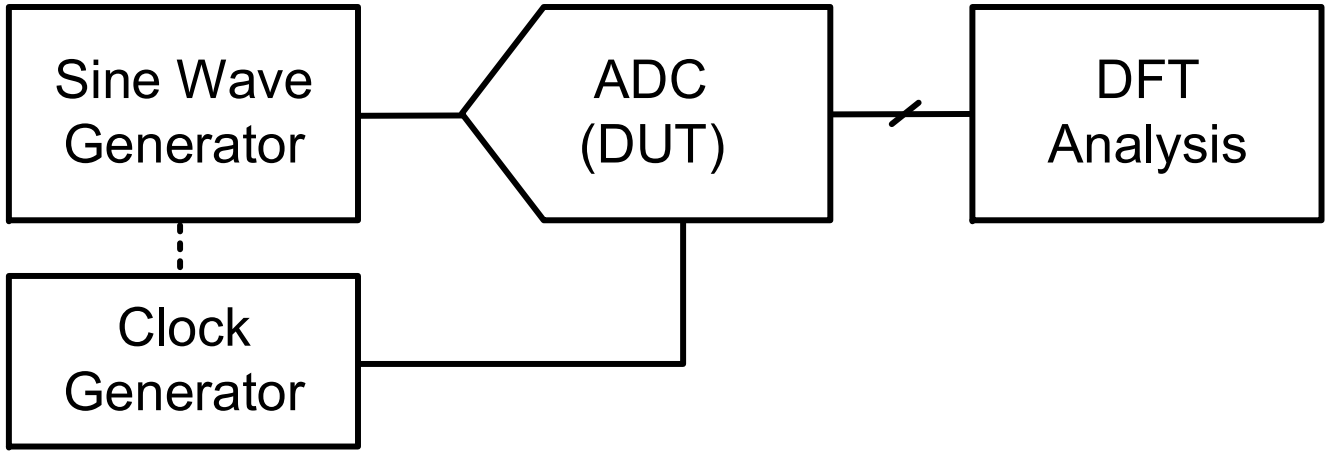
Static Performance Metrics





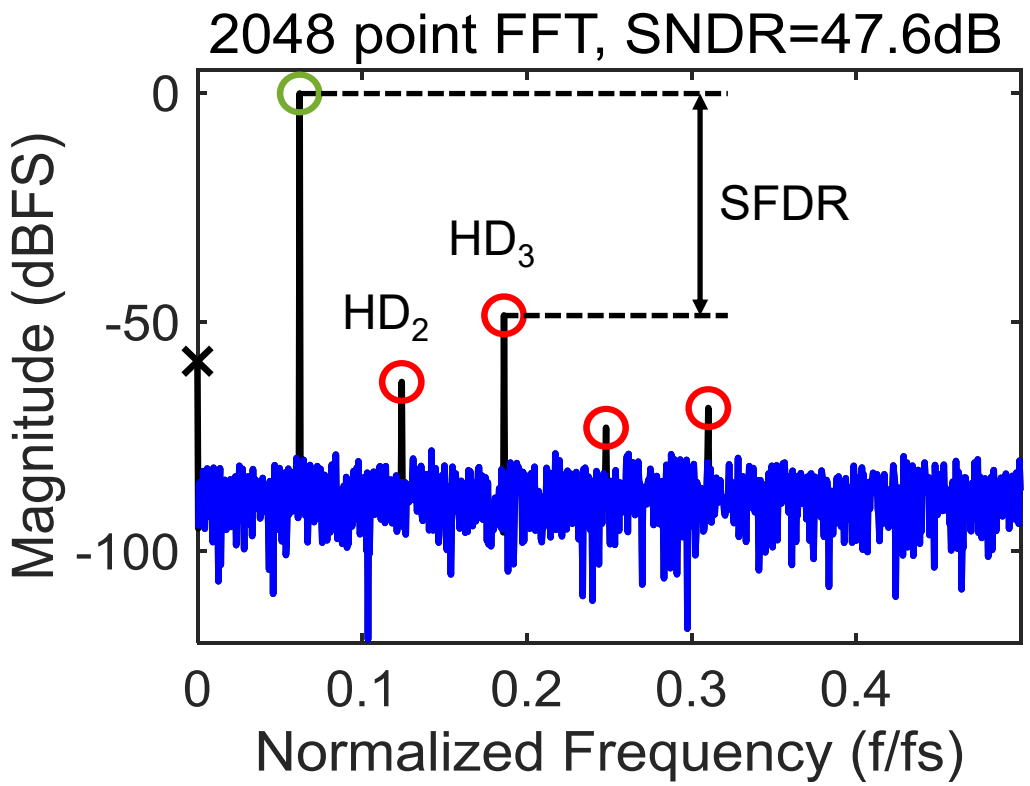
- Differential nonlinearity (DNL)
  - Relative errors in code width
- Integral nonlinearity (INL)
  - Decision level shifts relative to straight line → running sum of DNL

ADC Spectral Performance Analysis



- Discrete Fourier transform output lets us calculate several useful metrics
  - Signal-to-Noise Ratio (SNR)
  - Signal-to-Noise and Distortion Ratio (SNDR)
  - Spurious-Free-Dynamic Range (SFDR)
  - Harmonic Distortion (HD)

Basic Single-Tone Metrics for ADCs



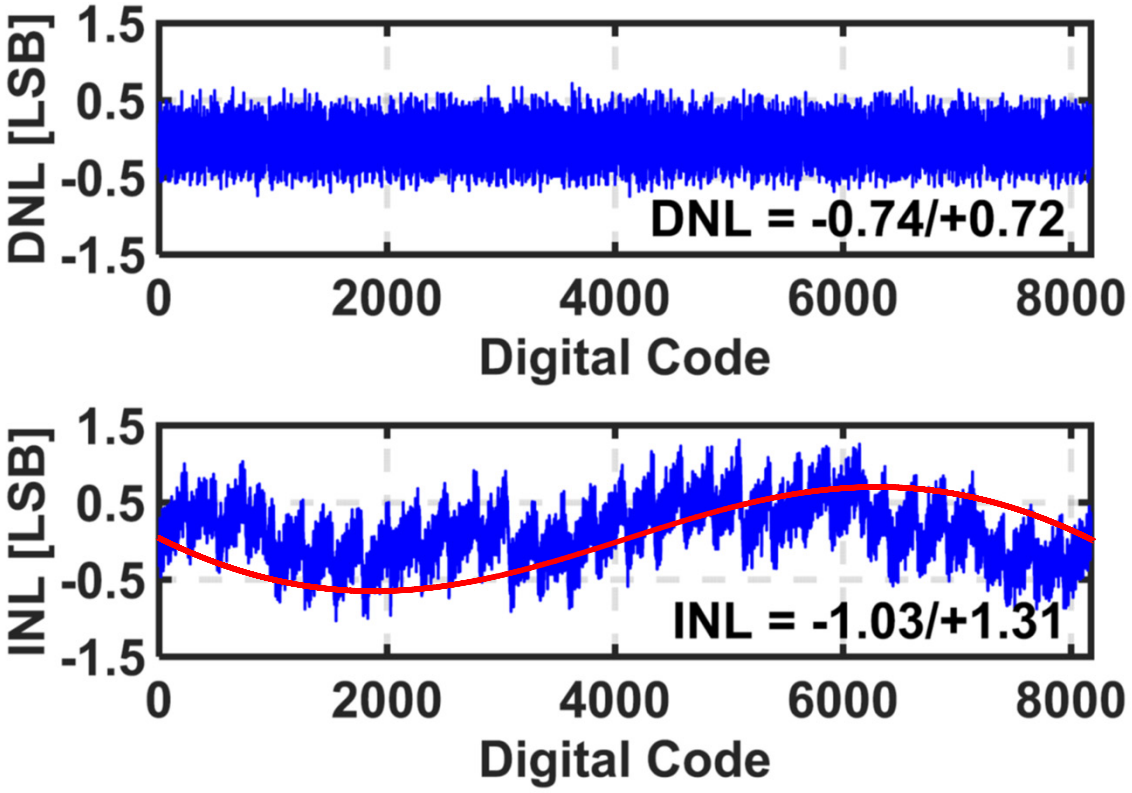
$$SNR = \frac{P_{Sig}}{P_{Noise}}$$

$$SNDR = \frac{P_{Sig}}{P_{Noise} + P_{HD}}$$

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02}$$

$$SFDR = \frac{P_{Sig}}{P_{largest\ spur}}$$

Relationship Between SFDR and INL



[Zhang, ISSCC 2019]

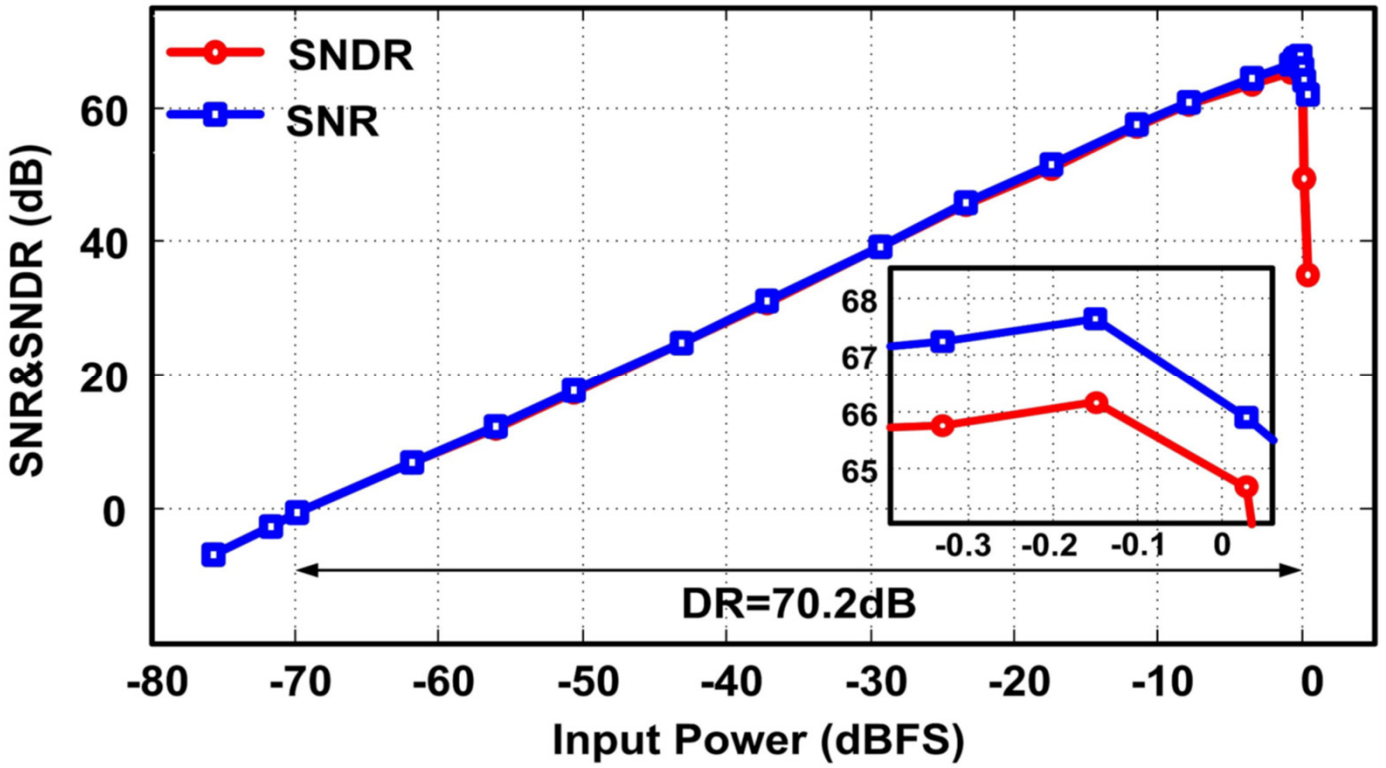
- INL often shows major transitions and cubic/quadratic bows
- For visible bows, we can roughly estimate SFDR using

$$SFDR \approx -20\,log\left(\frac{INL_{fit}}{2^B}\right)$$

$$SFDR \approx -20\,log\left(\frac{0.5}{2^{13}}\right) = 84\,dB$$

(Measured SFDR is 89 dB)

Dynamic Range (DR)

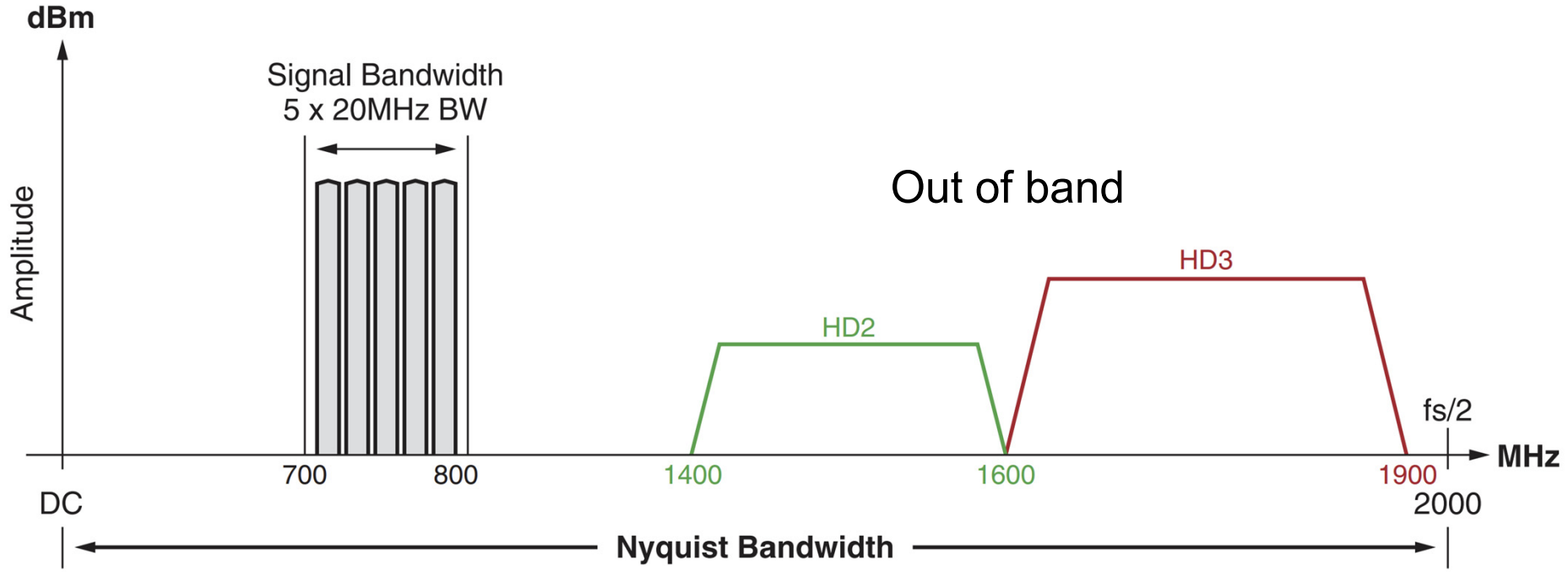


[Lin, ISSCC 2021]

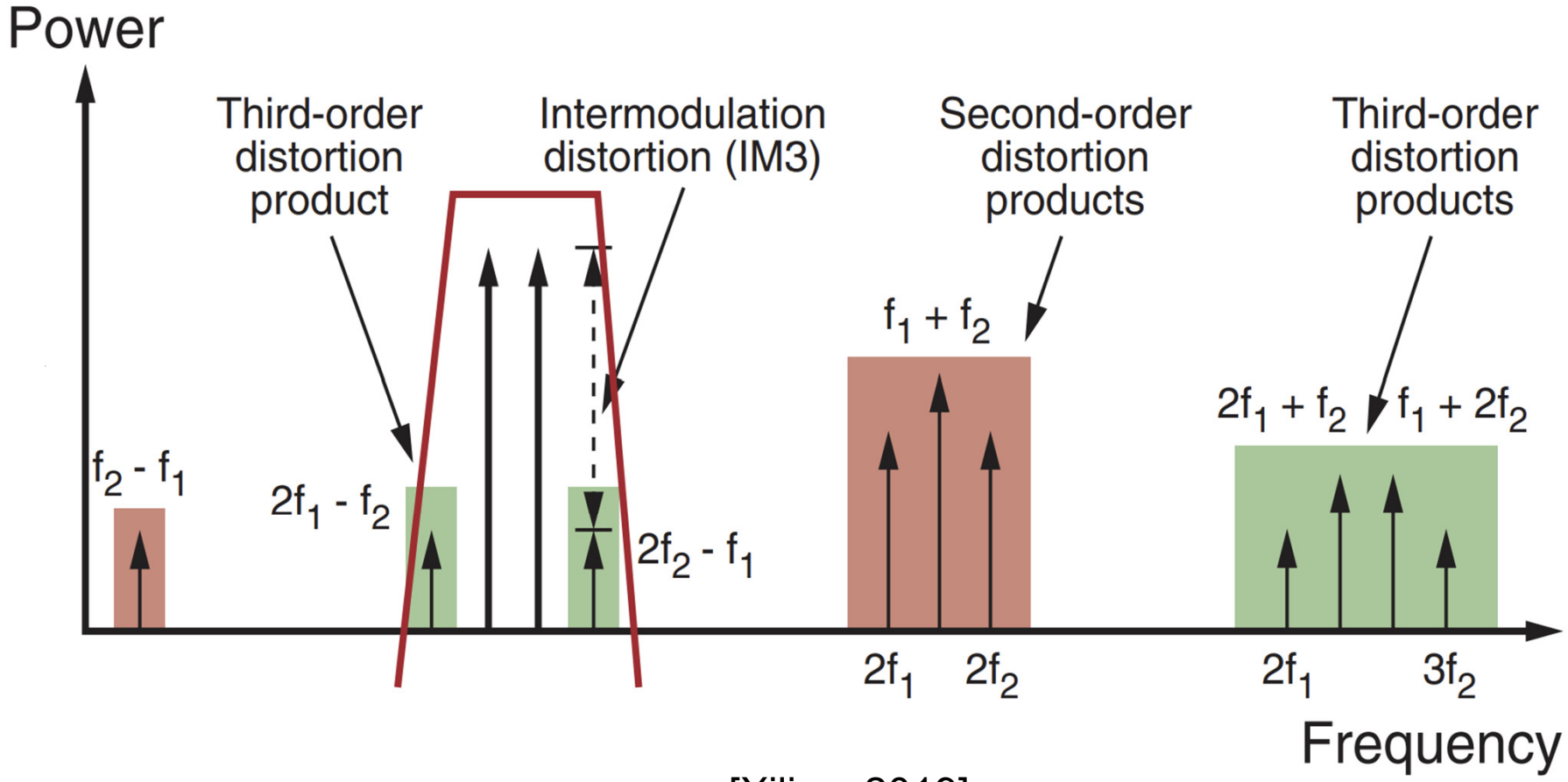
- Ratio of strongest and weakest signal (@SNR=0dB)
- DR ≥ Peak SNR, SNDR

The Need for Advanced Metrics

- Consider RF ADC for LTE [Xilinx, 2019]
- Single-tone metrics like SFDR are irrelevant



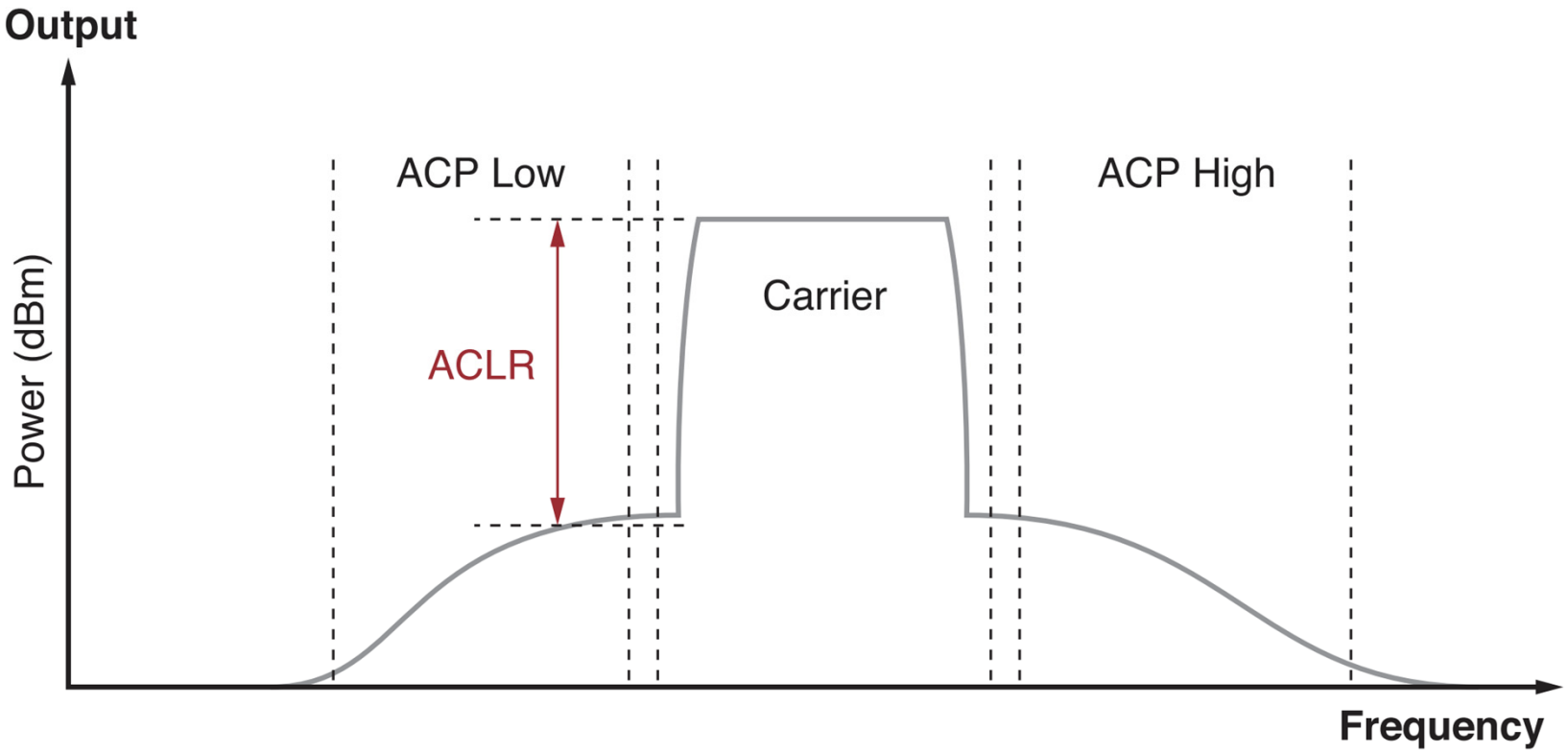
Two-Tone Test



[Xilinx, 2019]

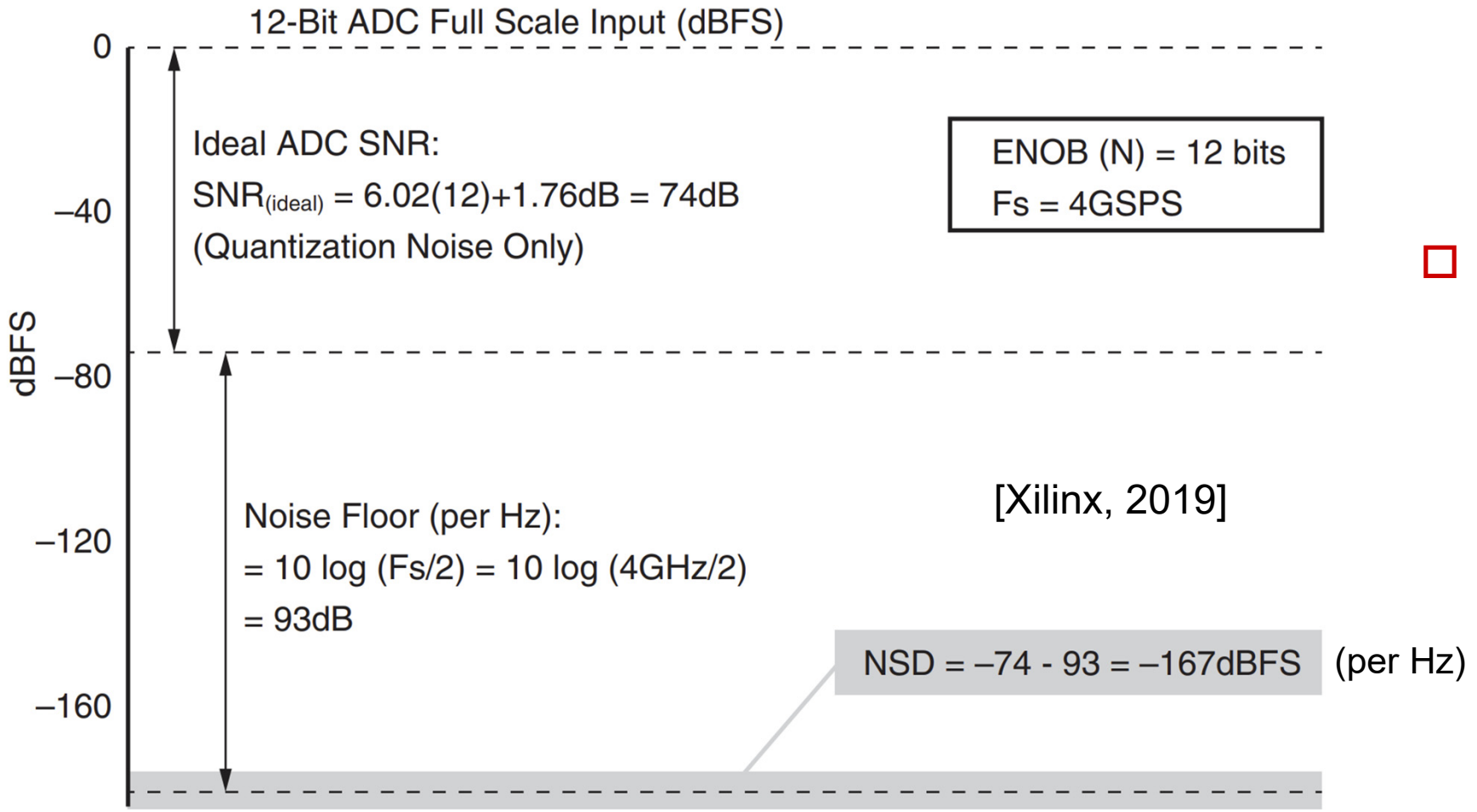
Adjacent Channel Leakage Ratio (ACLR)

- Ratio of modulated signal power and power leaked into adjacent channels



[Xilinx, 2019]

Noise Spectral Density (NSD)



[Xilinx, 2019]

- Useful for estimating in-band noise within a fraction of the Nyquist band

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  - Application aspects

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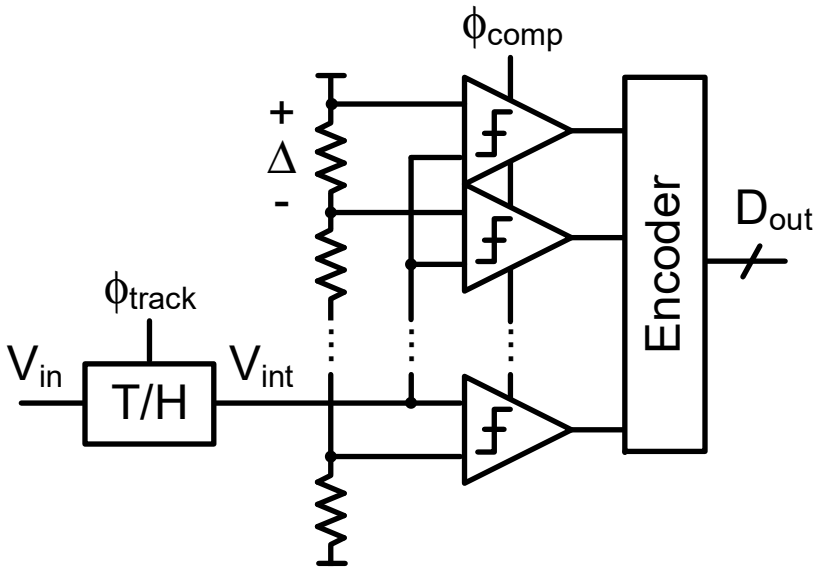
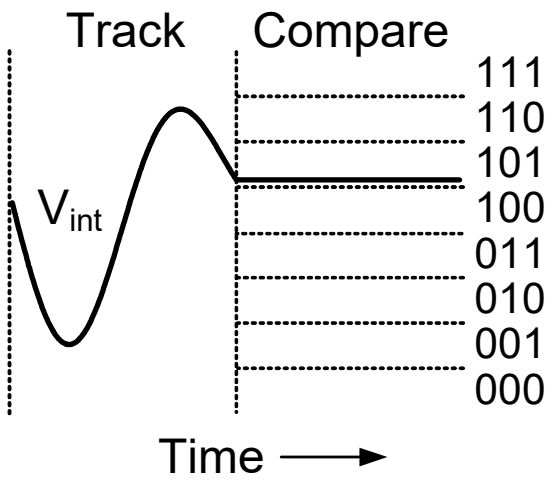
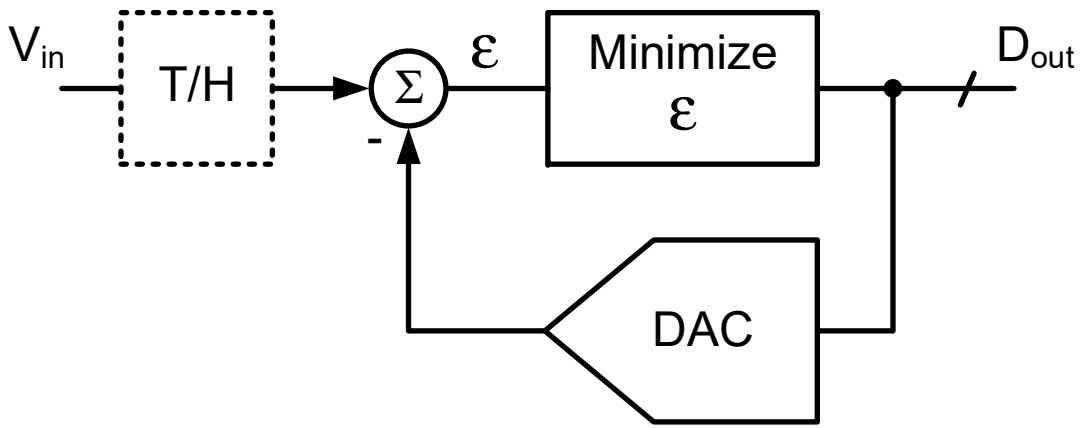
Rudimentary Architecture: Flash ADC





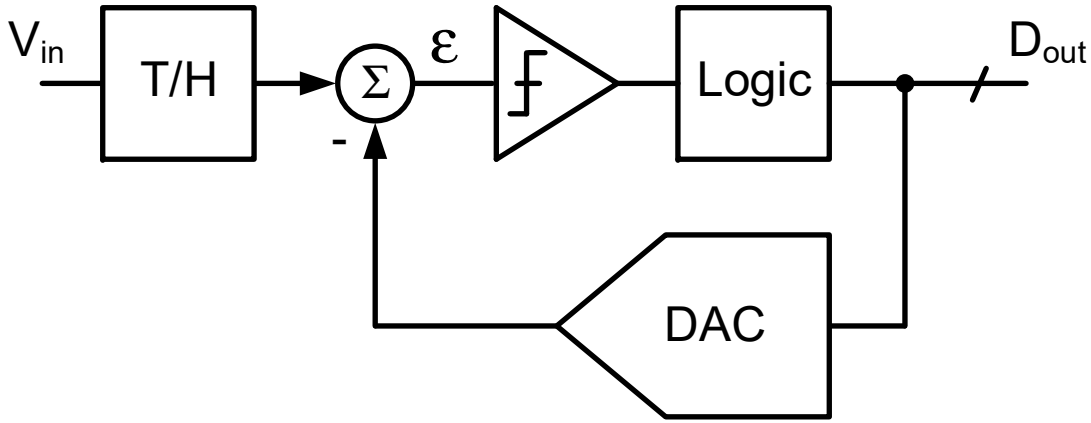
- Compare sampled input to all decision levels in parallel
- Fast, but requires 2^B-1 comparators
- Typically use for B≤6
  - Managing comparator offset becomes major challenge for larger B

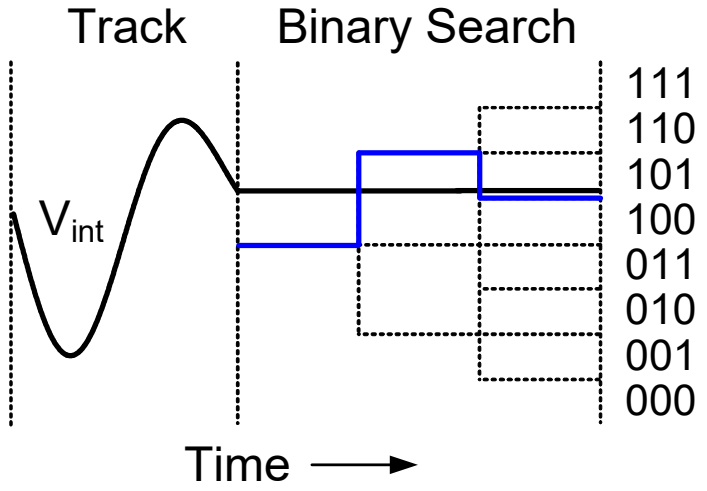
Essence of Most Other ADC Architectures



- Fidelity typically limited by circuits connected to summing node
- DAC is usually a major pain point
  - Especially in CT ΔΣ modulators

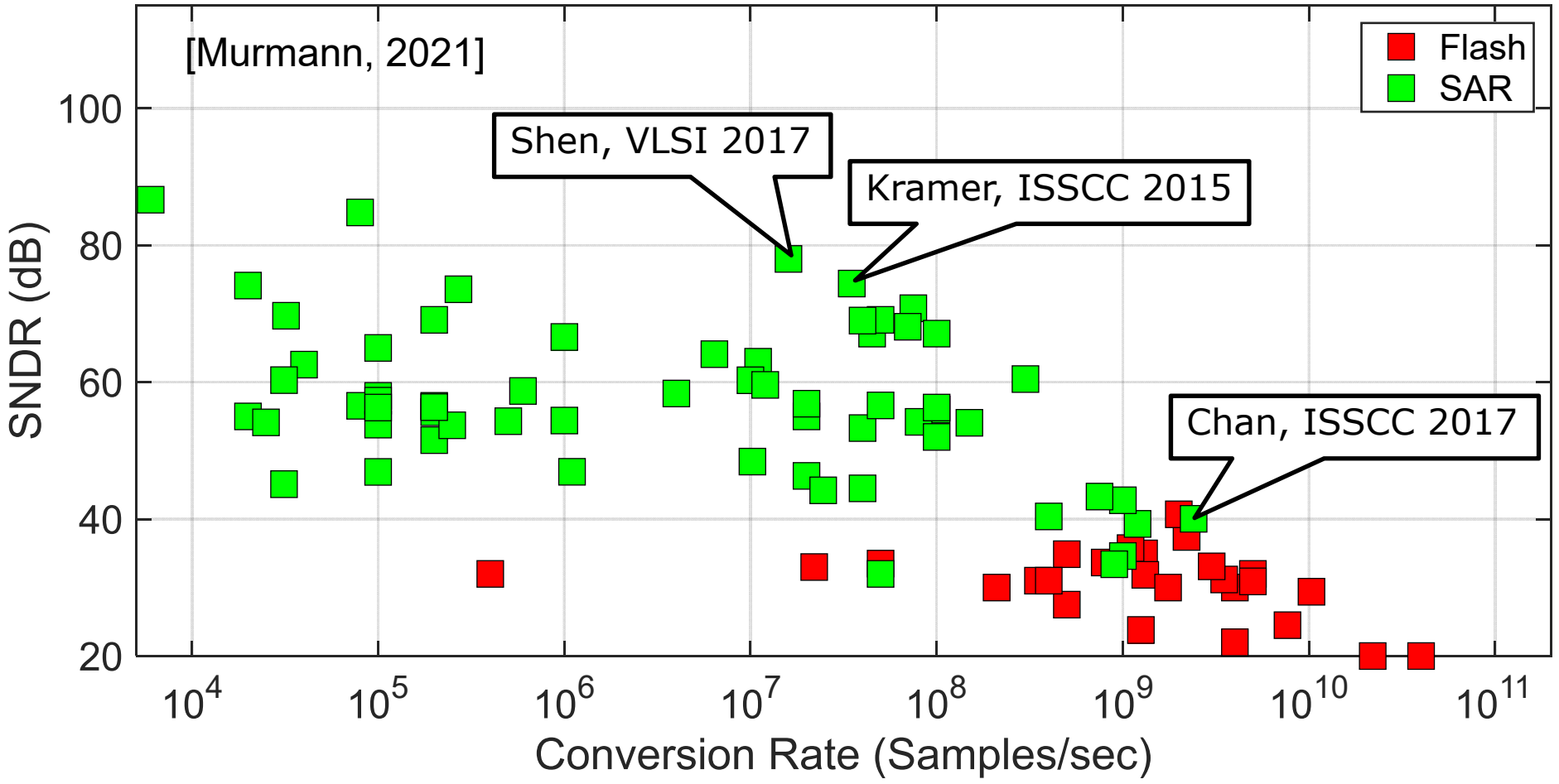
Successive Approximation Register ADC





- Usually employ only one comparator
- Bits are determined sequentially; conversion time increases ~B
- Linearity determined by sub-DAC
- Comparator noise a significant issue for B>10
  - Can introduce redundancy to relax specs (see Pieter Harpe's talk)

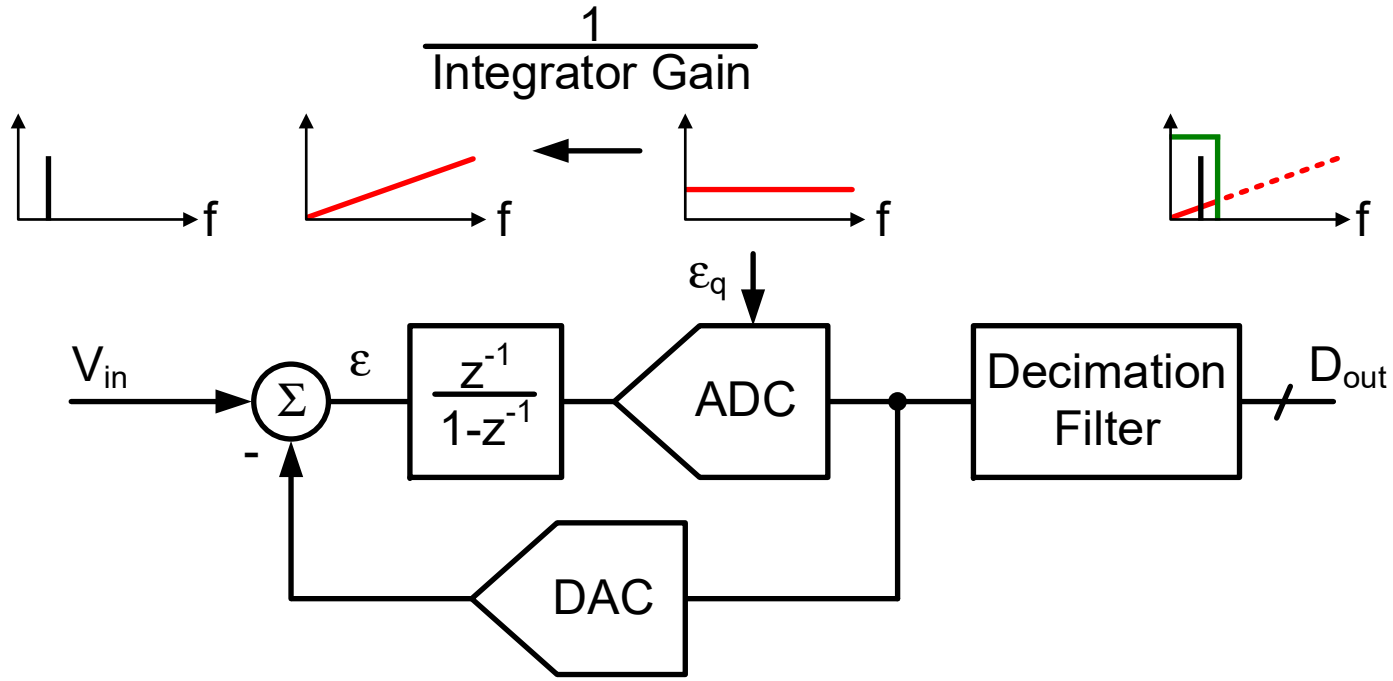
Published Data (ISSCC & VLSI Symposium)



Pushing the Envelope

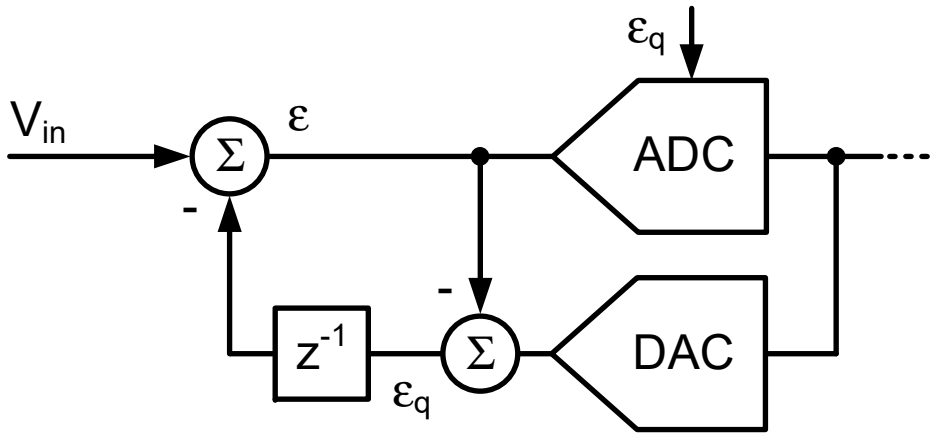
- Higher resolution
  - Oversampling and noise shaping ($\Delta\Sigma$ modulators)
- Higher speed
  - Pipelining
  - Time interleaving
- Current trend
  - Mixing and matching all the above options, and across all architectures
  - "Hybrid ADCs"

Oversampling and Noise Shaping



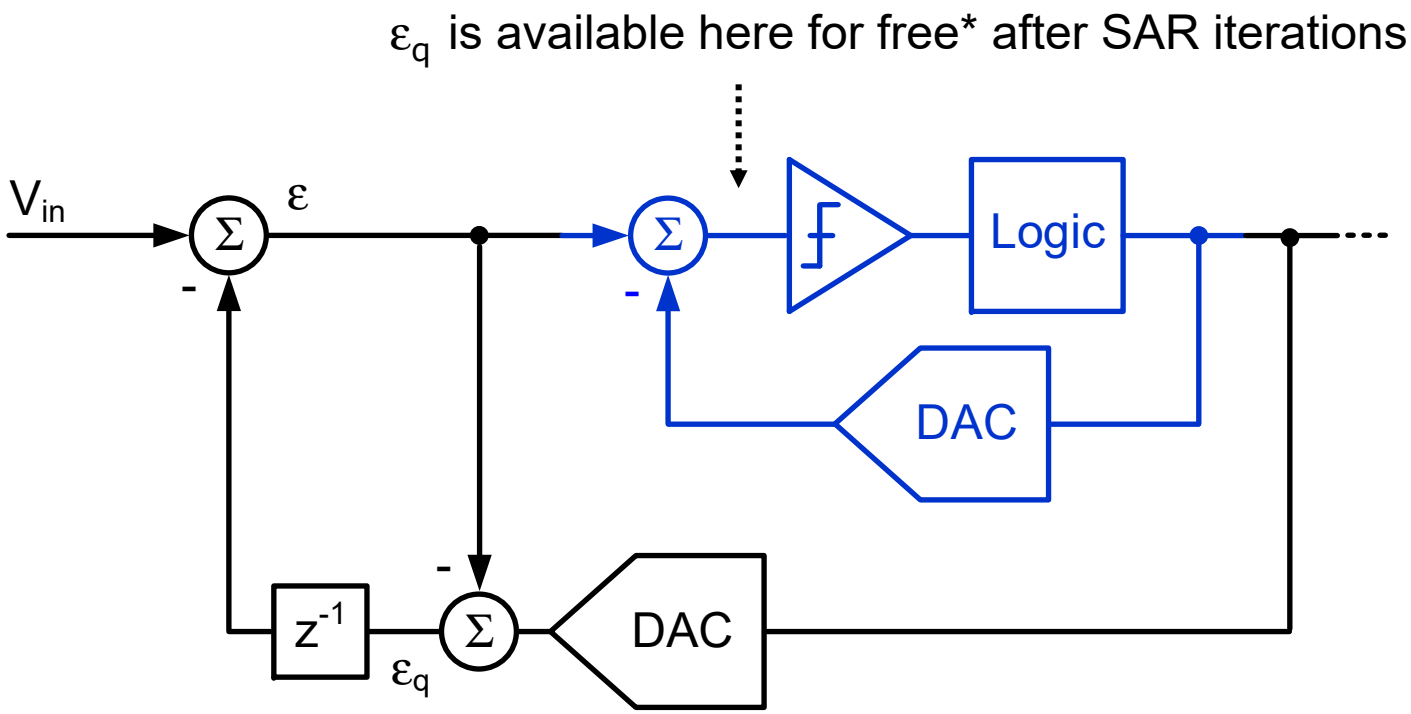
- Integrator forces ε to zero near DC
- Many variants exist (DT/CT, high-order loop filters, bandpass, …)
- Performance typically set by DAC and first stage of loop filter

Equivalent Model Using Error Feedback



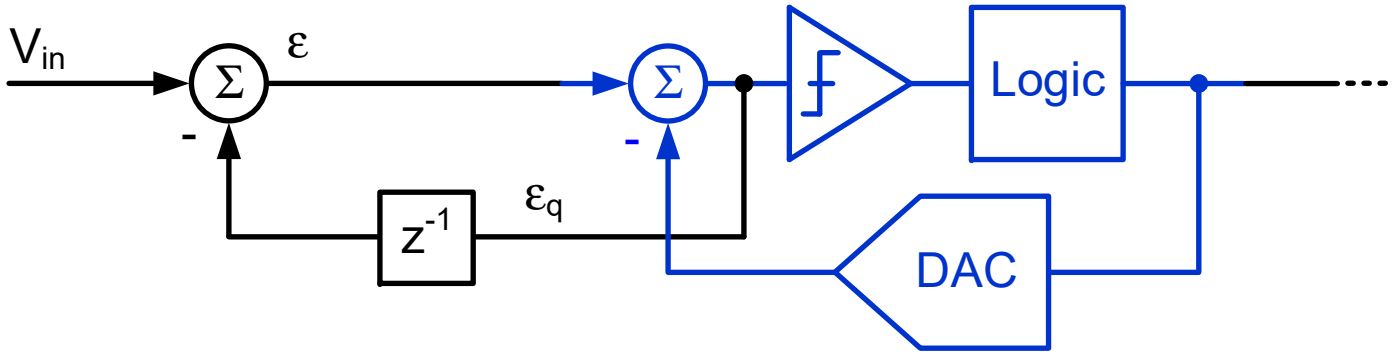
- Quantization error from previous input is subtracted from current input ($1-z^{-1}$)
  - Highpass filtering as shown on previous slide
- Previously used only for $\Delta\Sigma$ DACs, due to high feedback coefficient sensitivity
  - But, workable for low-order with high-resolution quantizers
  - First noise shaping SAR ADC by [Fredenburg & Flynn, ISSCC 2012]

Plugging in a SAR ADC



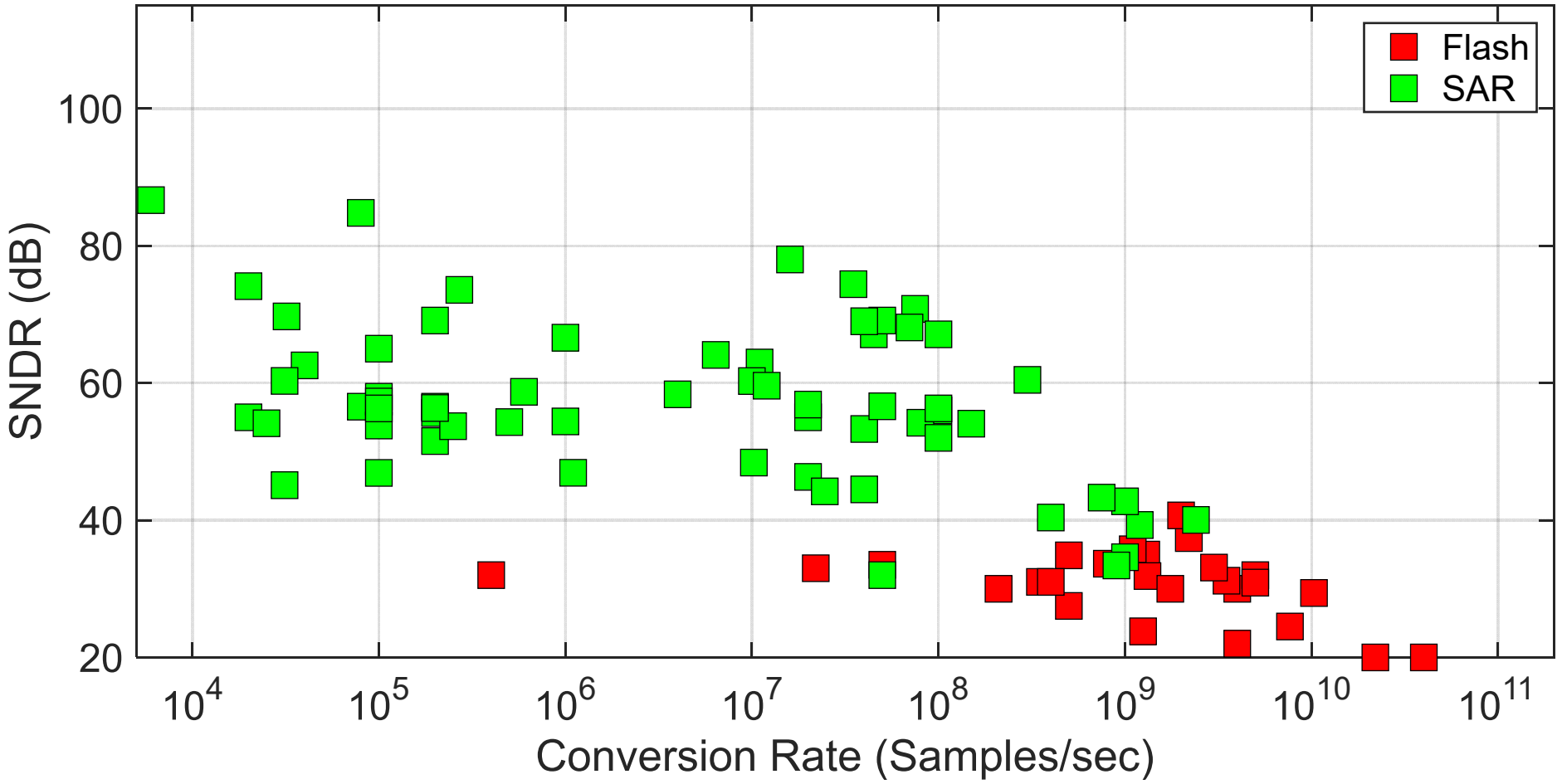
*Typically need to run an extra cycle to feed back final bit decision

Plugging in a SAR ADC

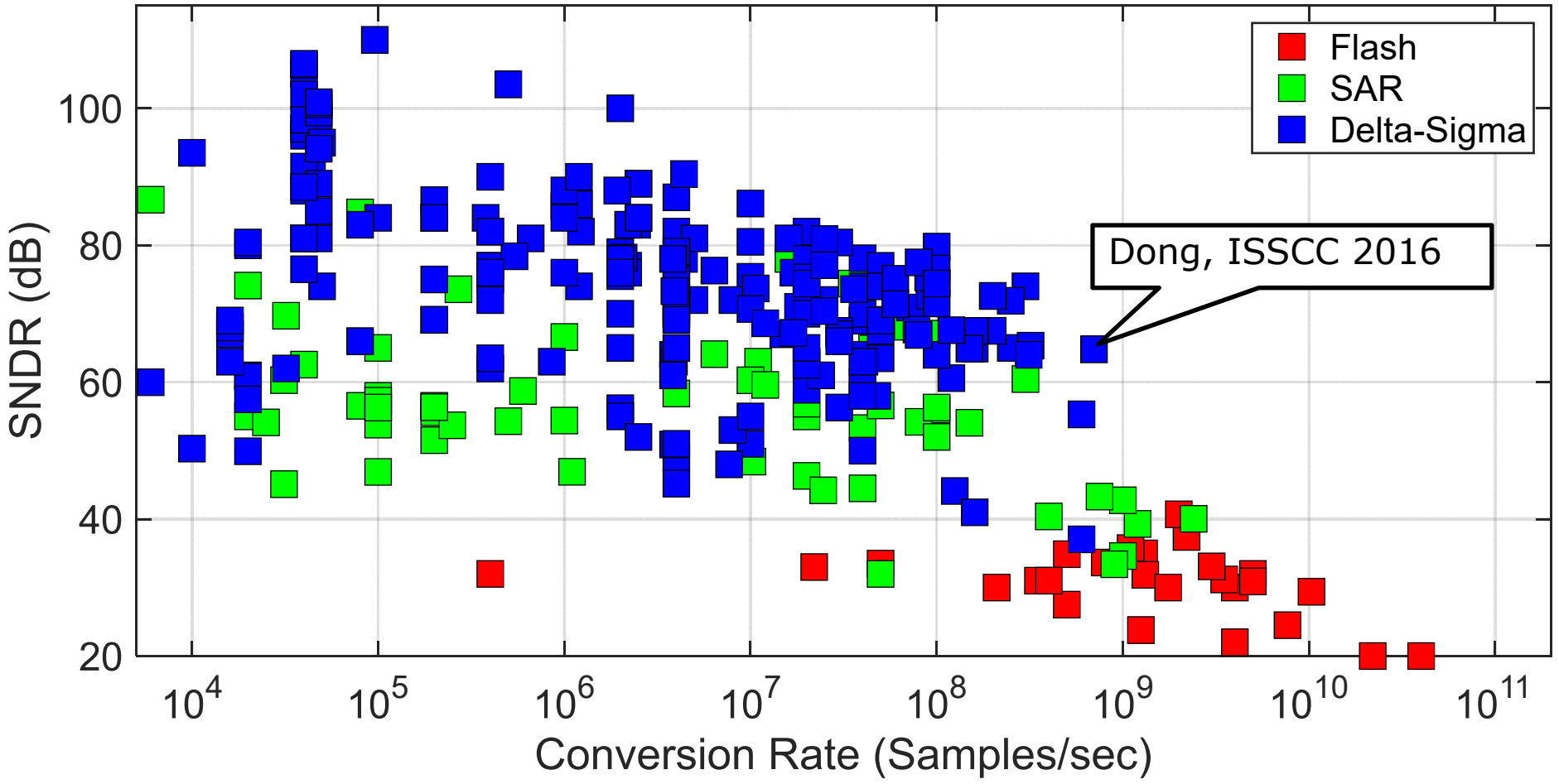


- Key is to find an efficient circuit realization that minimizes active components and allows for extensions such as second-order noise shaping
  - See e.g. [Li & Sun, ISSCC 2018]; more in Nan Sun's presentation

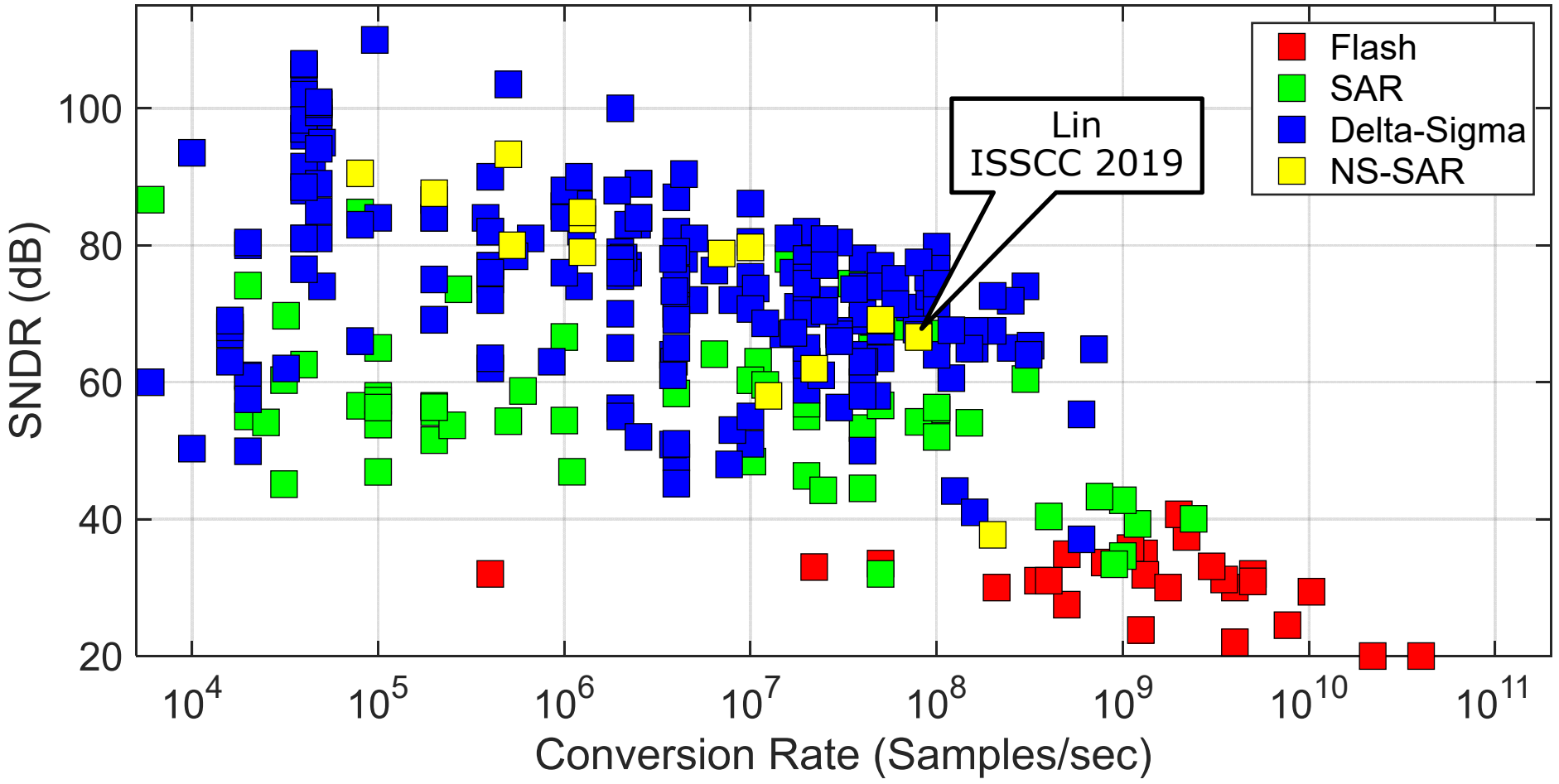
Published Data (ISSCC & VLSI Symposium)



Adding "Standard" ΔΣ ADCs



Adding Noise-Shaped SAR ADCs



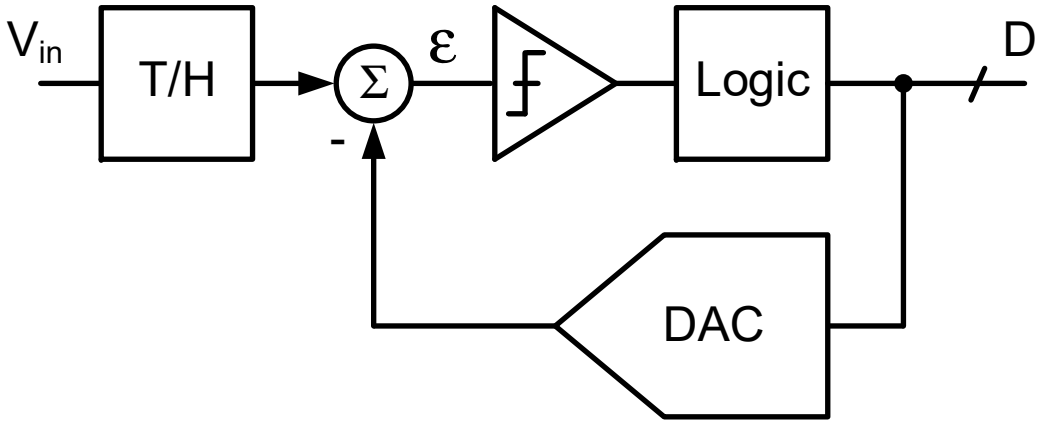
Higher Speed Through Pipelining

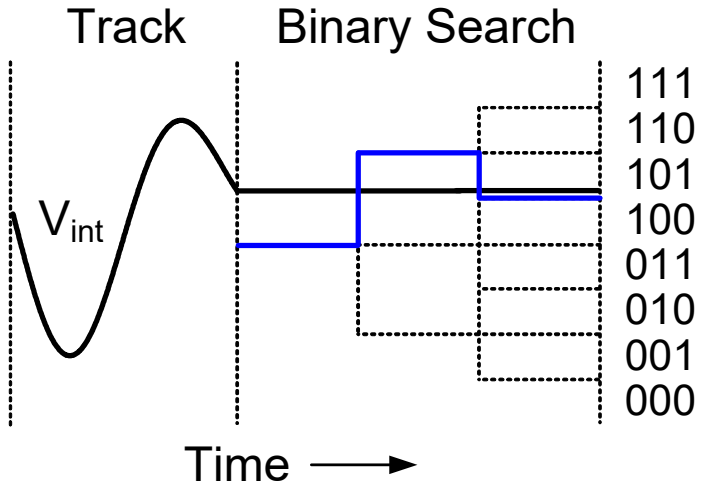
Ford assembly line in 1913
[Wikimedia Commons]

- Determine bits sequentially (as in a SAR ADC)
- But use concurrent "workers" (stages)
- Throughput set by one worker
- Latency set by number of workers

	Cycles per Conversion	**Complexity**
Flash	~1	$\sim 2^B$
Pipeline	~1	~B
SAR	~B	~1

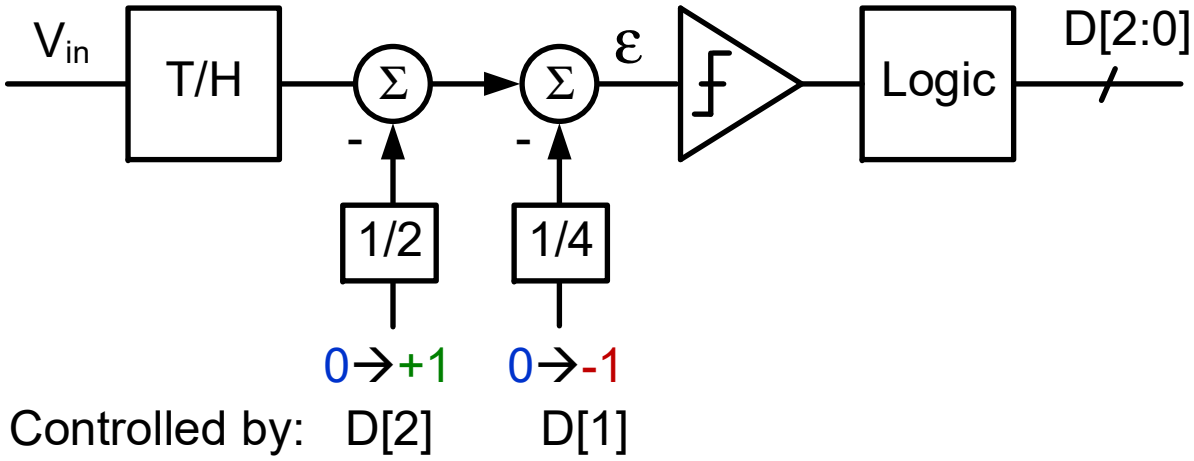
From SAR to Pipeline (1)

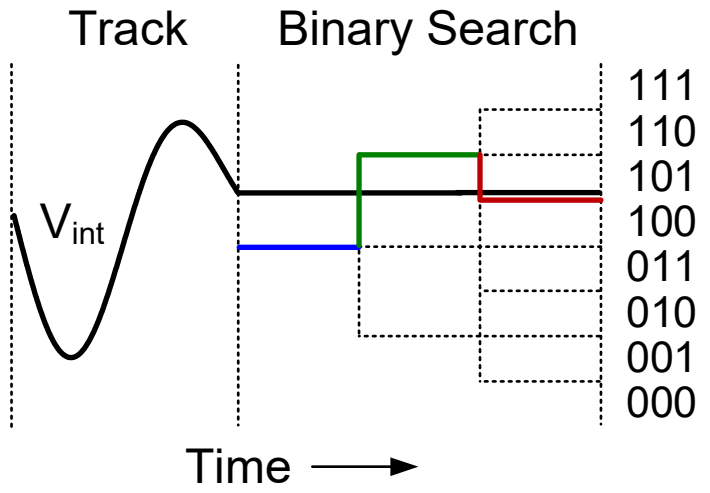




- We can morph a SAR ADC into a pipeline by
  - Distributing the DAC across stages
  - Replicating the comparator in each stage
- Means that all known "calibration/correction tricks" apply to both topologies!

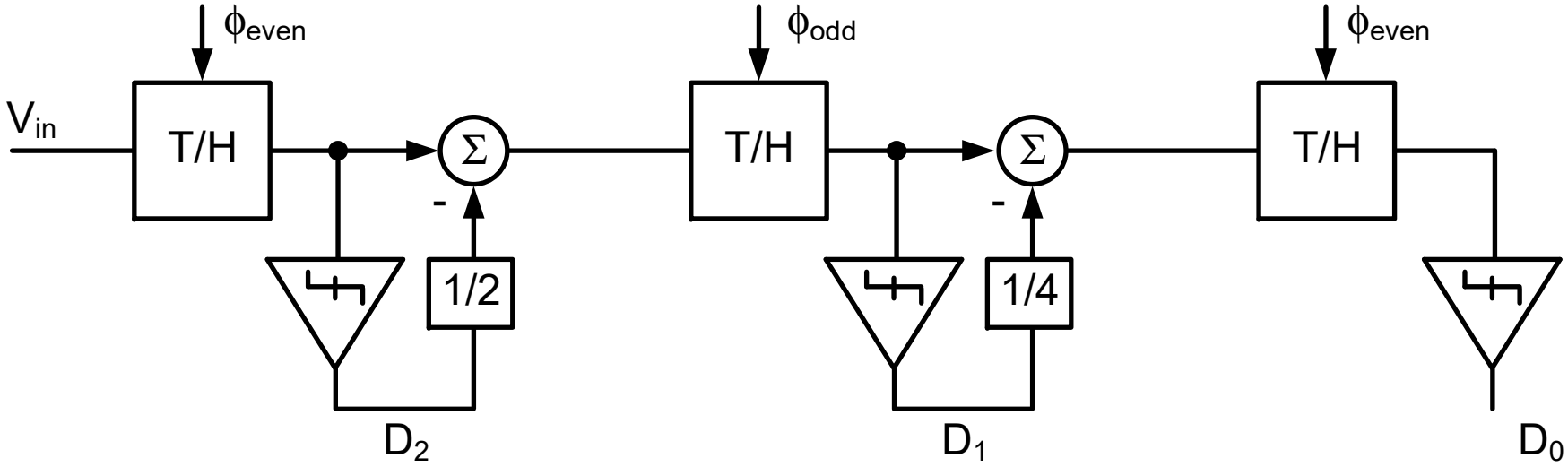
From SAR to Pipeline (2)





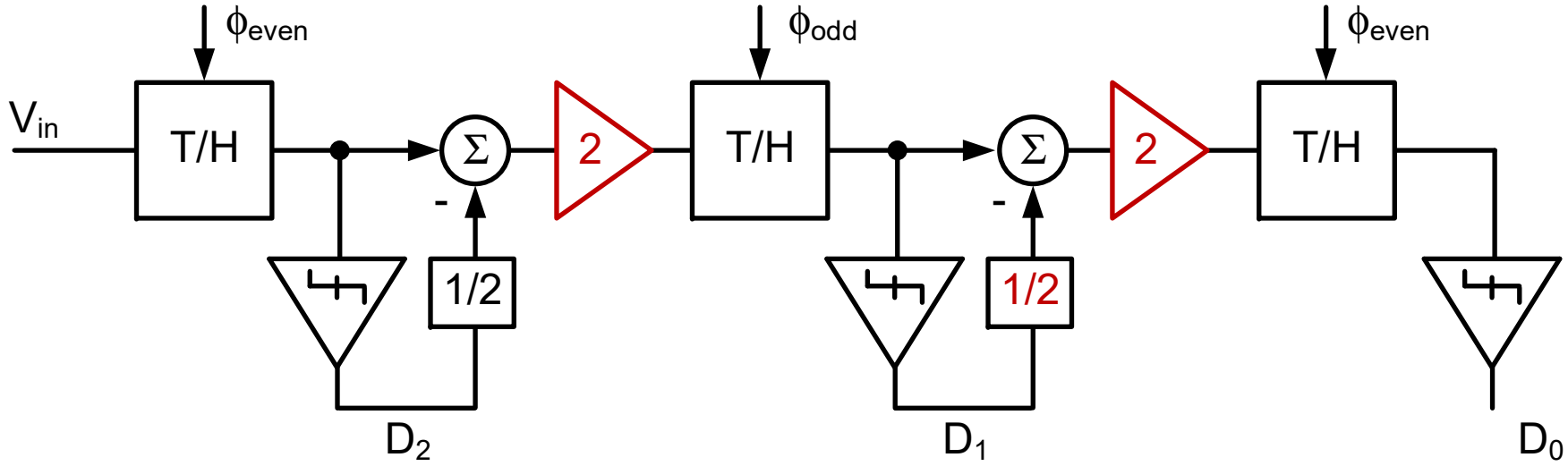
- Equivalent model with DAC broken up into its binary weights

From SAR to Pipeline (3)



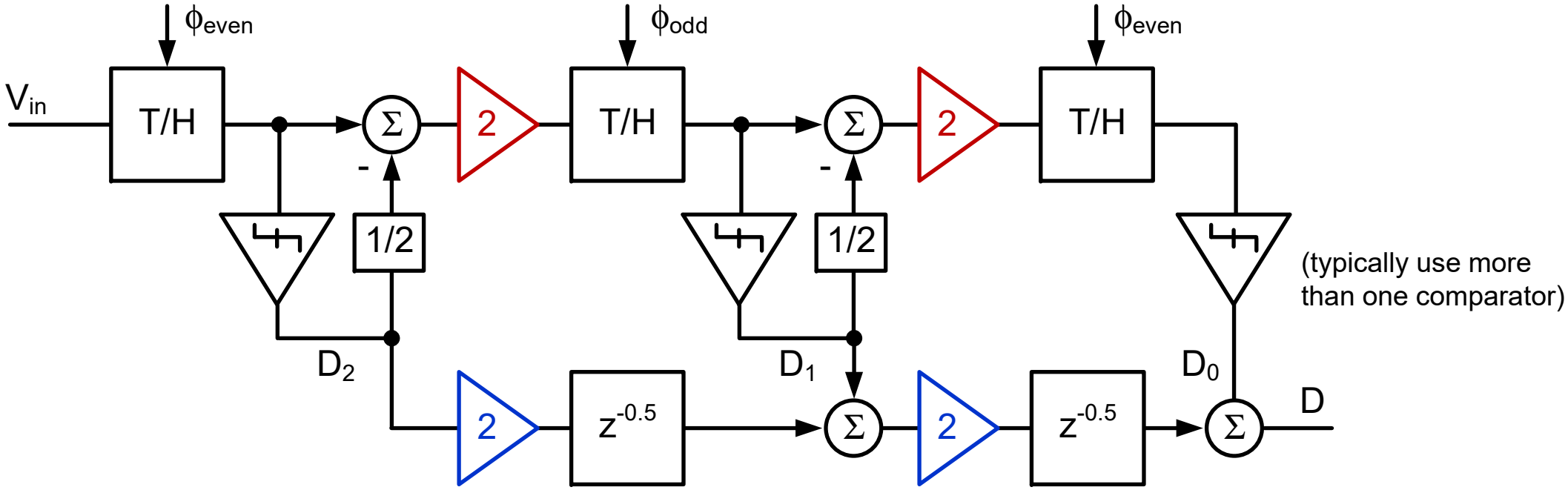
ϕ_{even}:	ACQUIRE	CONVERT	ACQUIRE
ϕ_{odd}:	CONVERT	ACQUIRE	CONVERT

From SAR to Pipeline (4)



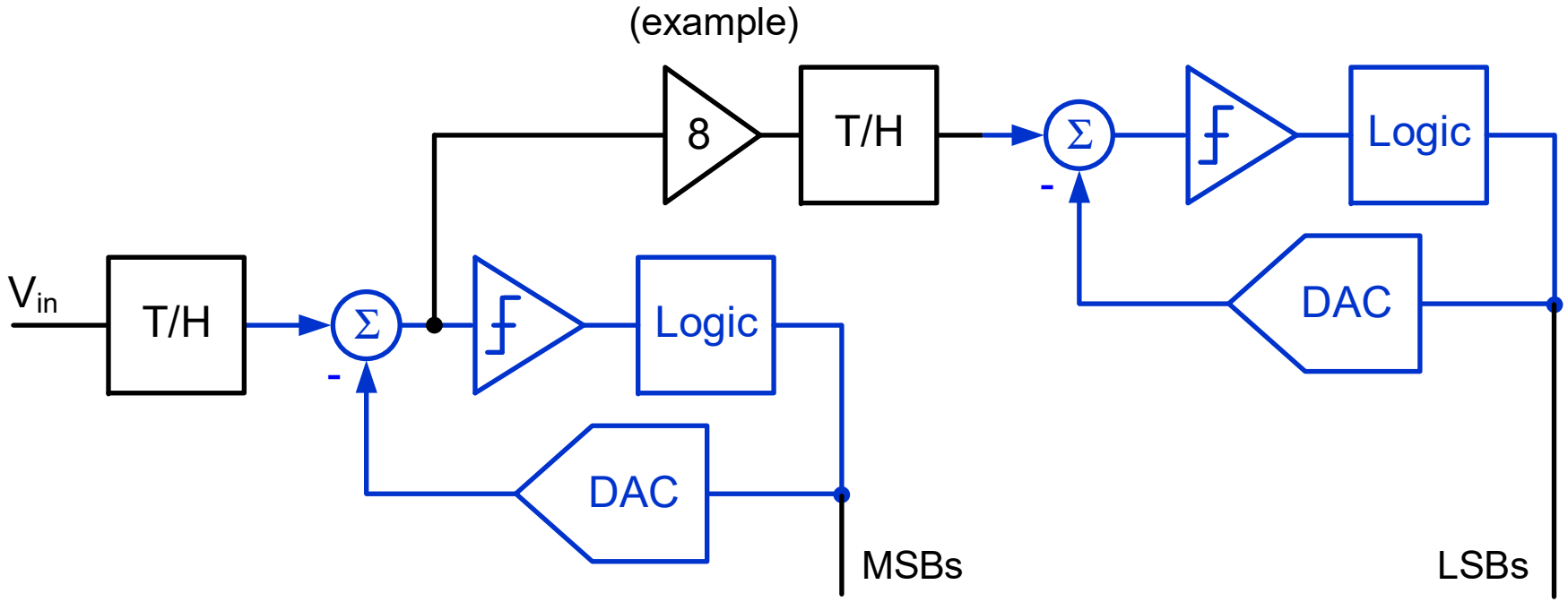
- Typically want to amplify residues back to full-scale to ease downstream circuit requirements

From SAR to Pipeline (5)



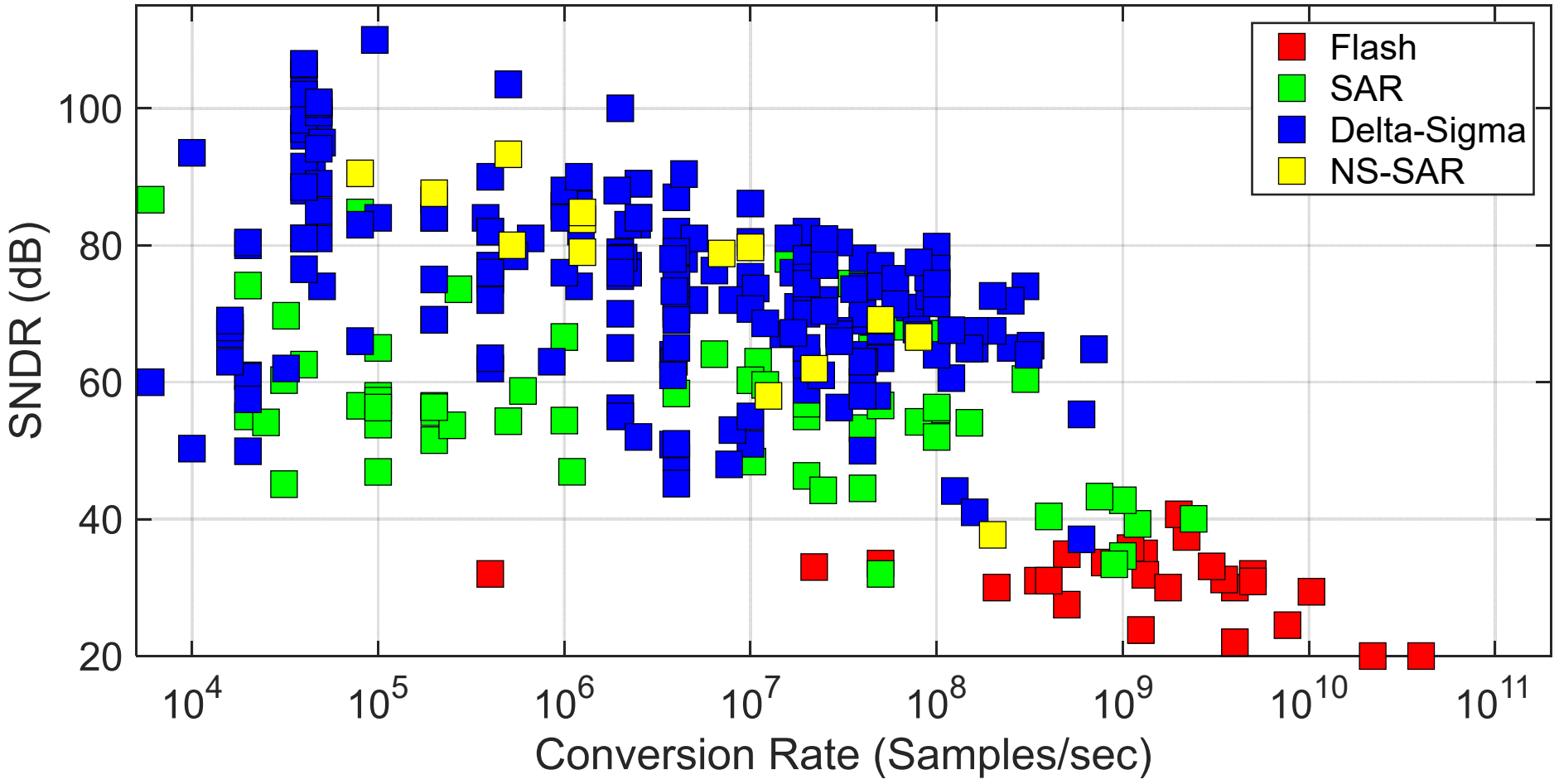
- Matching analog and digital front-end gains is a key issue
- Sometimes addressed through calibration

Pipelining SAR ADCs (!)

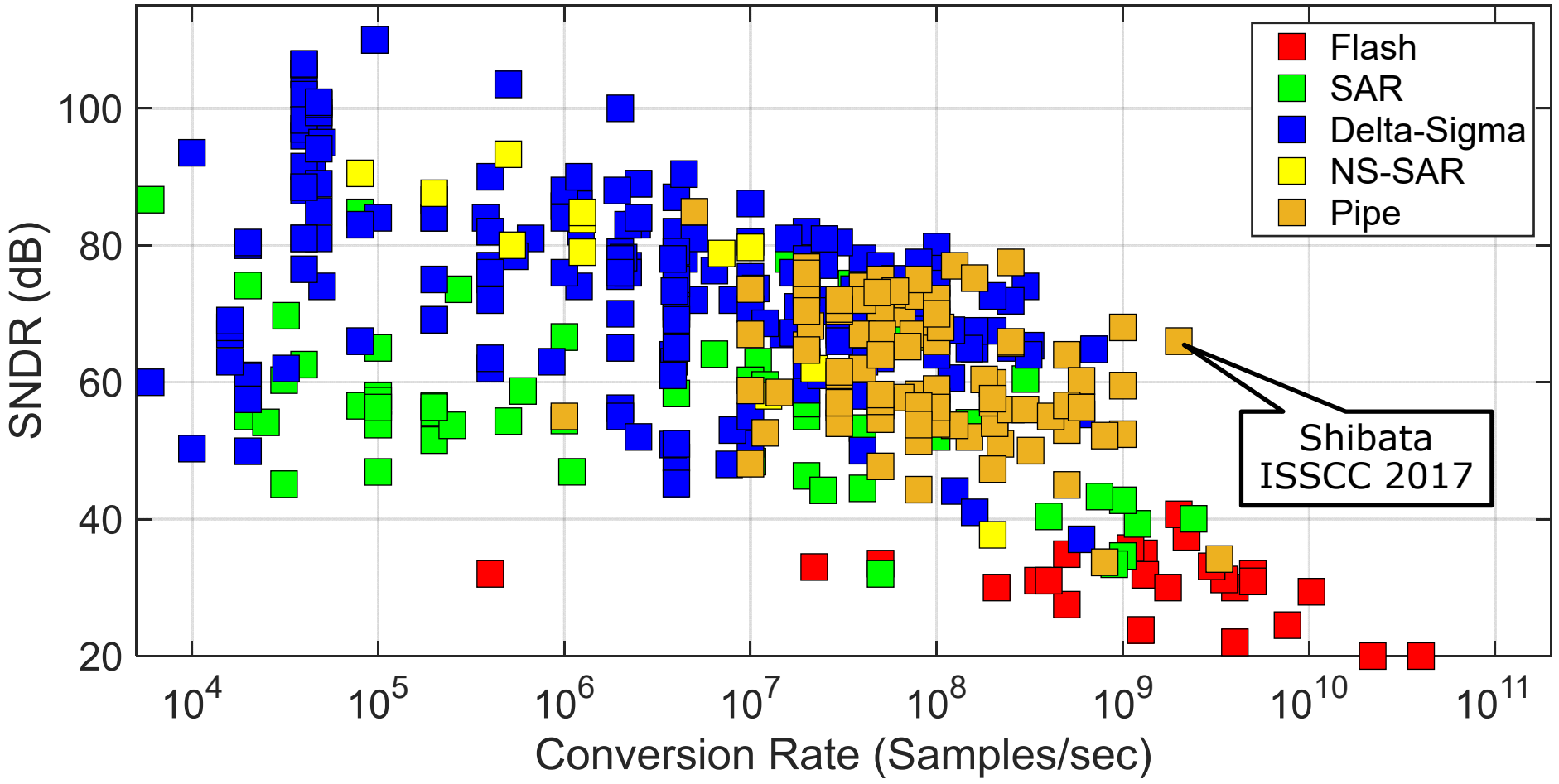


- Common to resolve more than one bit per stage in a pipeline
  - Conventionally this has been done using flash sub-ADCs
  - But SARs have become an attractive alternative
    - Can tap residue at comparator input

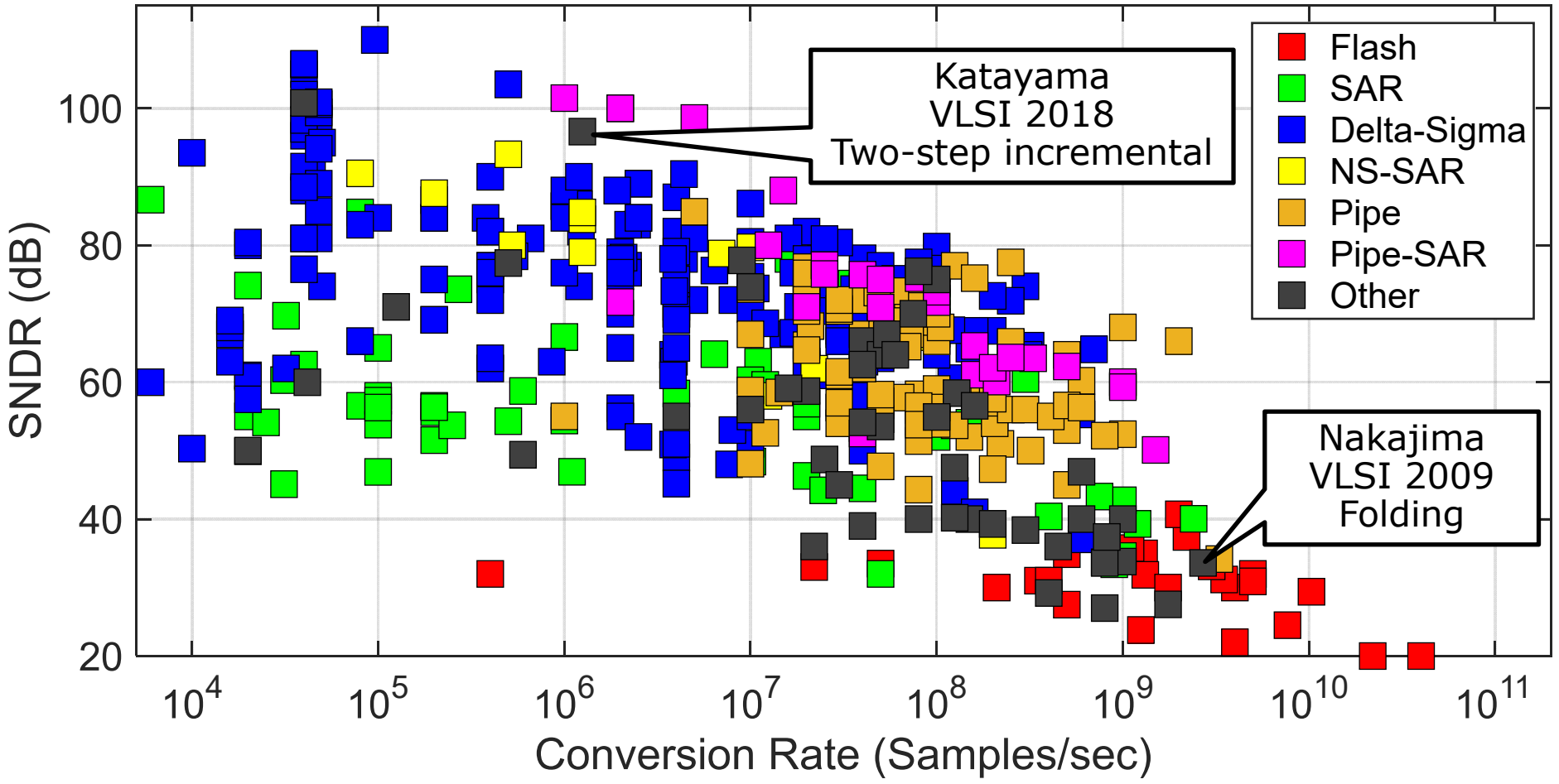
Published Data



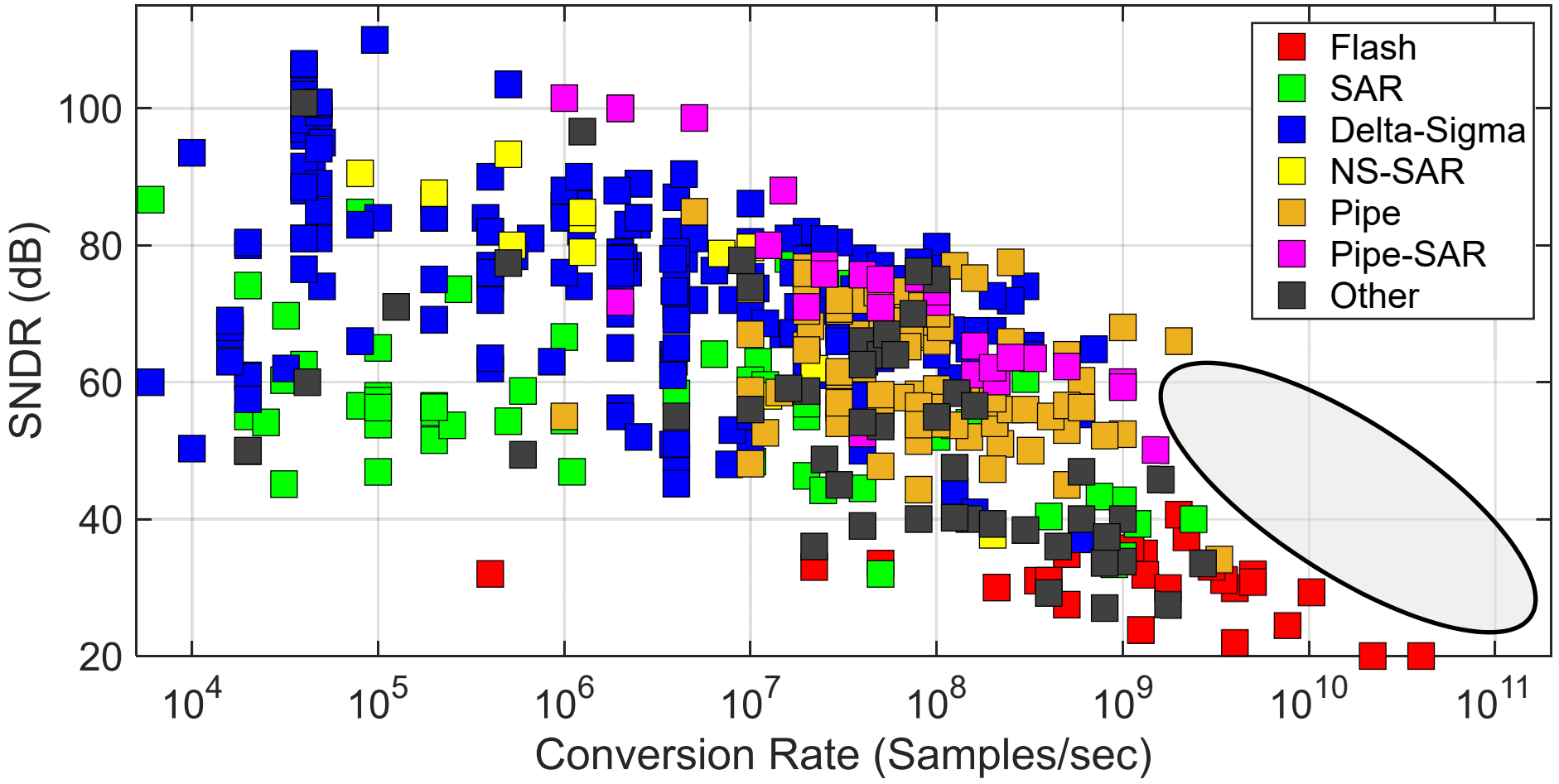
Adding Pipelined ADCs



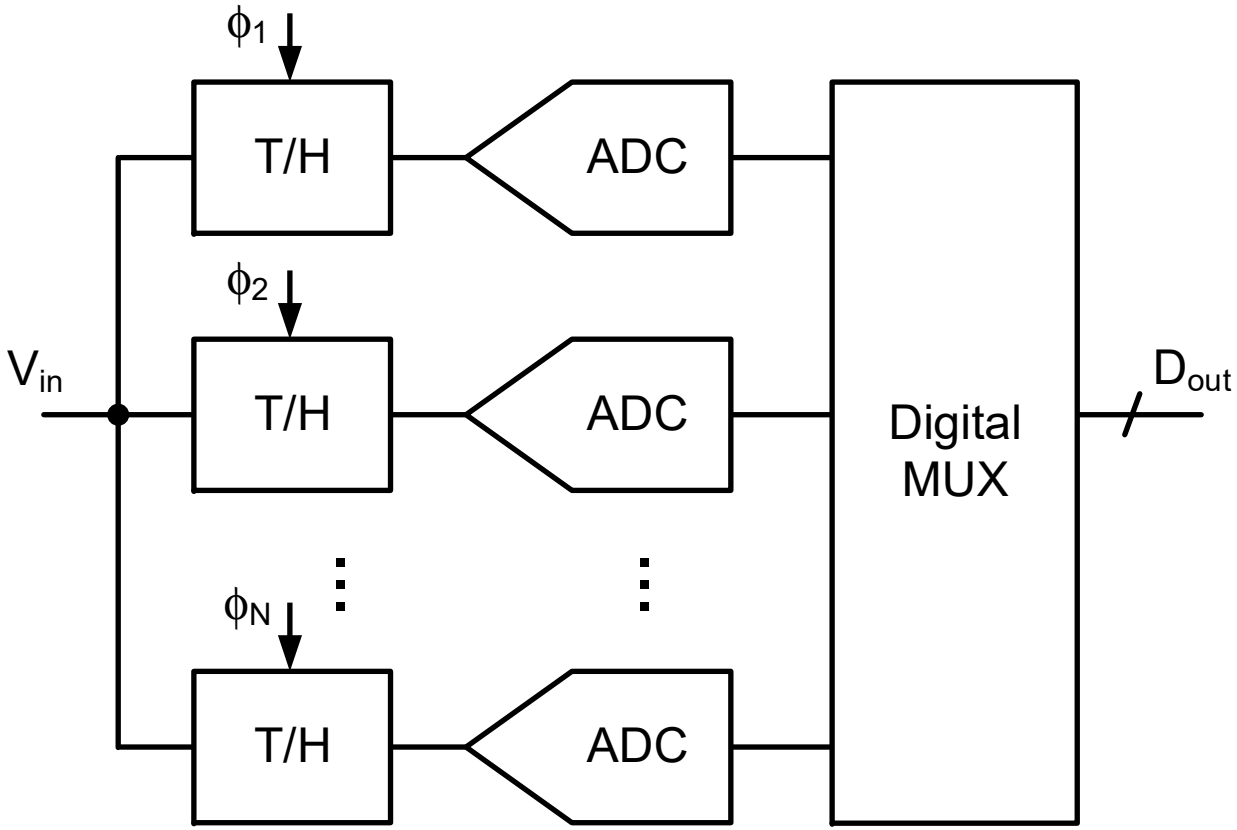
Adding “Other” Architectures



The Need for Time-Interleaving

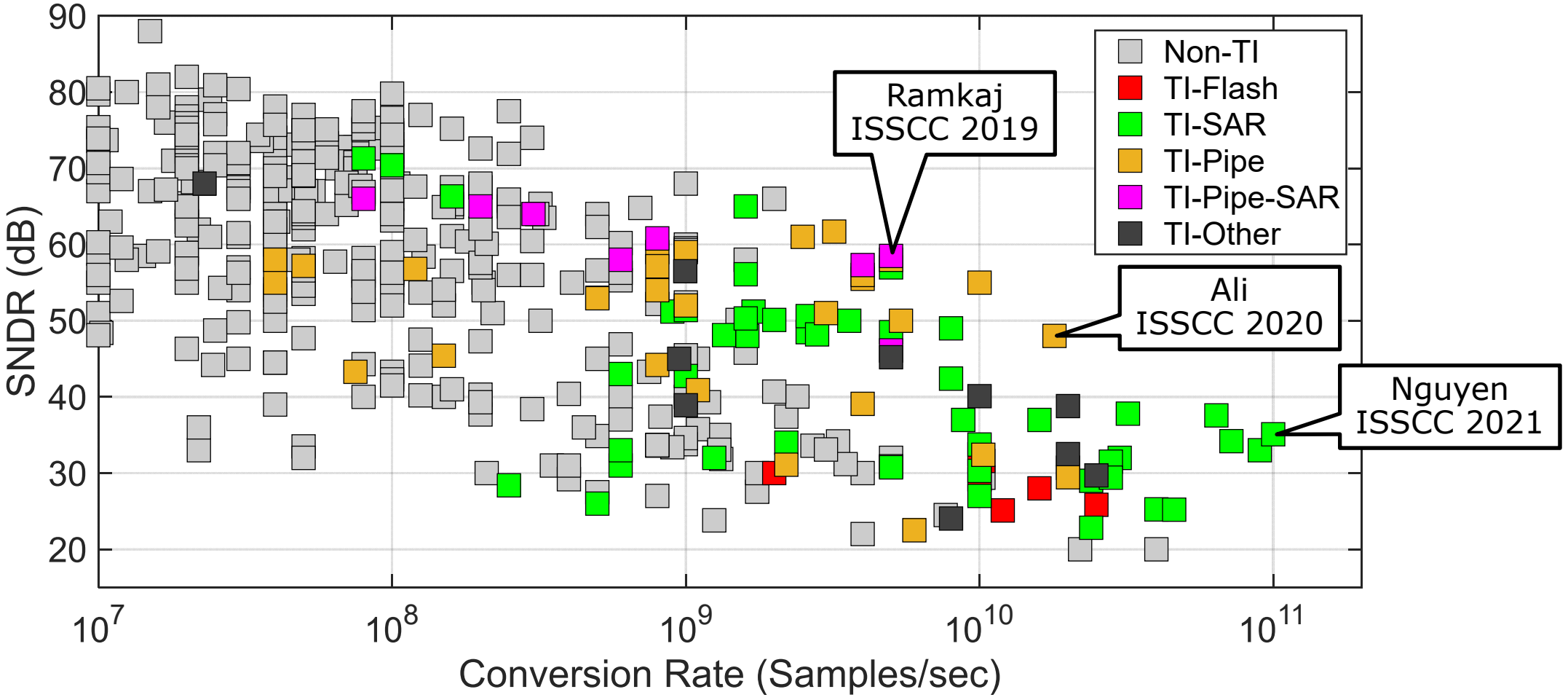


Time Interleaving

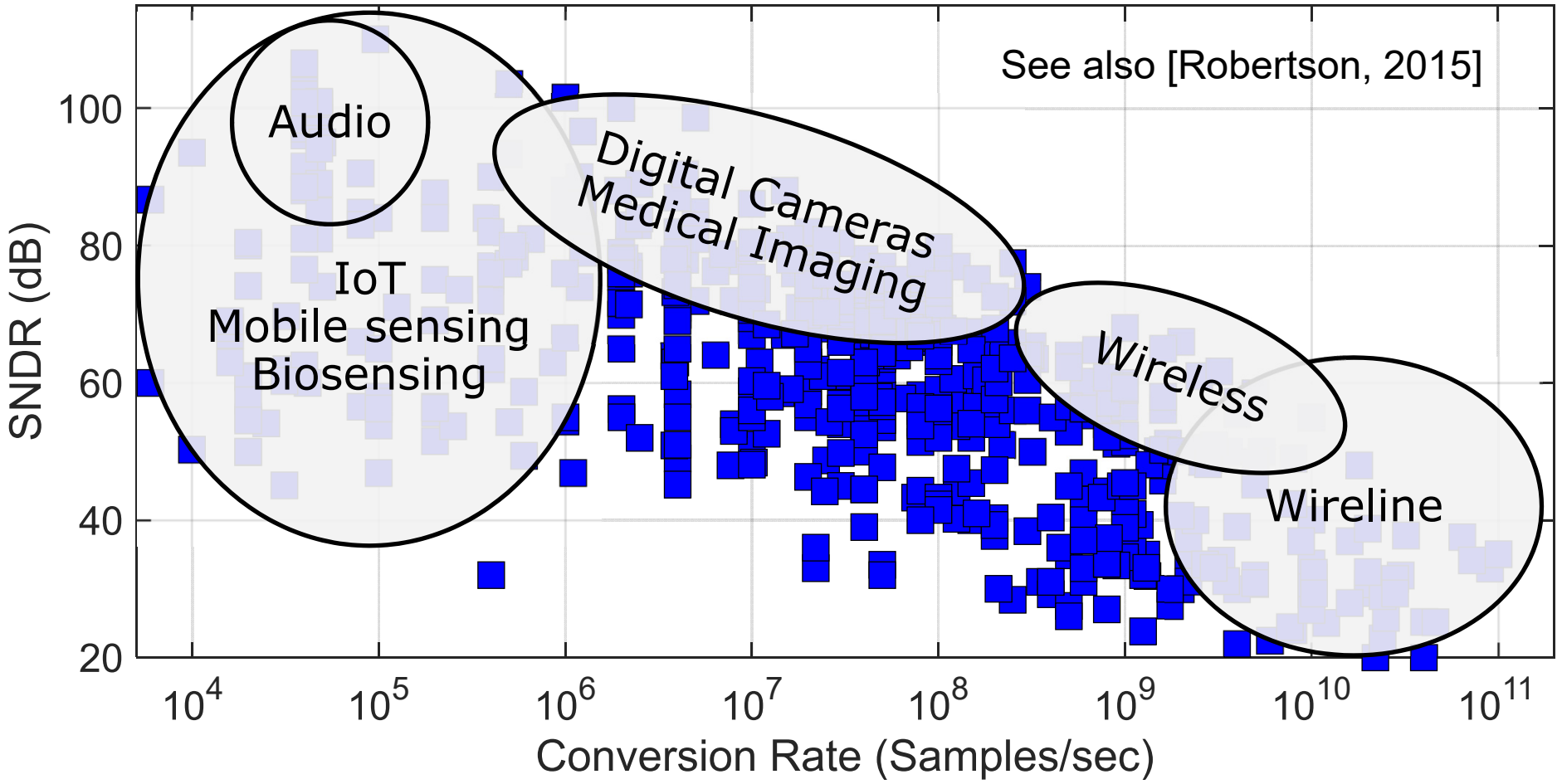


- N-fold increase in conversion rate
  - But each slice needs full acquisition bandwidth
- Sensitive to channel mismatches
  - Offset
  - Gain
  - Timing
  - Bandwidth
- Architectural variations
  - Global T/H
  - Hierarchical interleaving

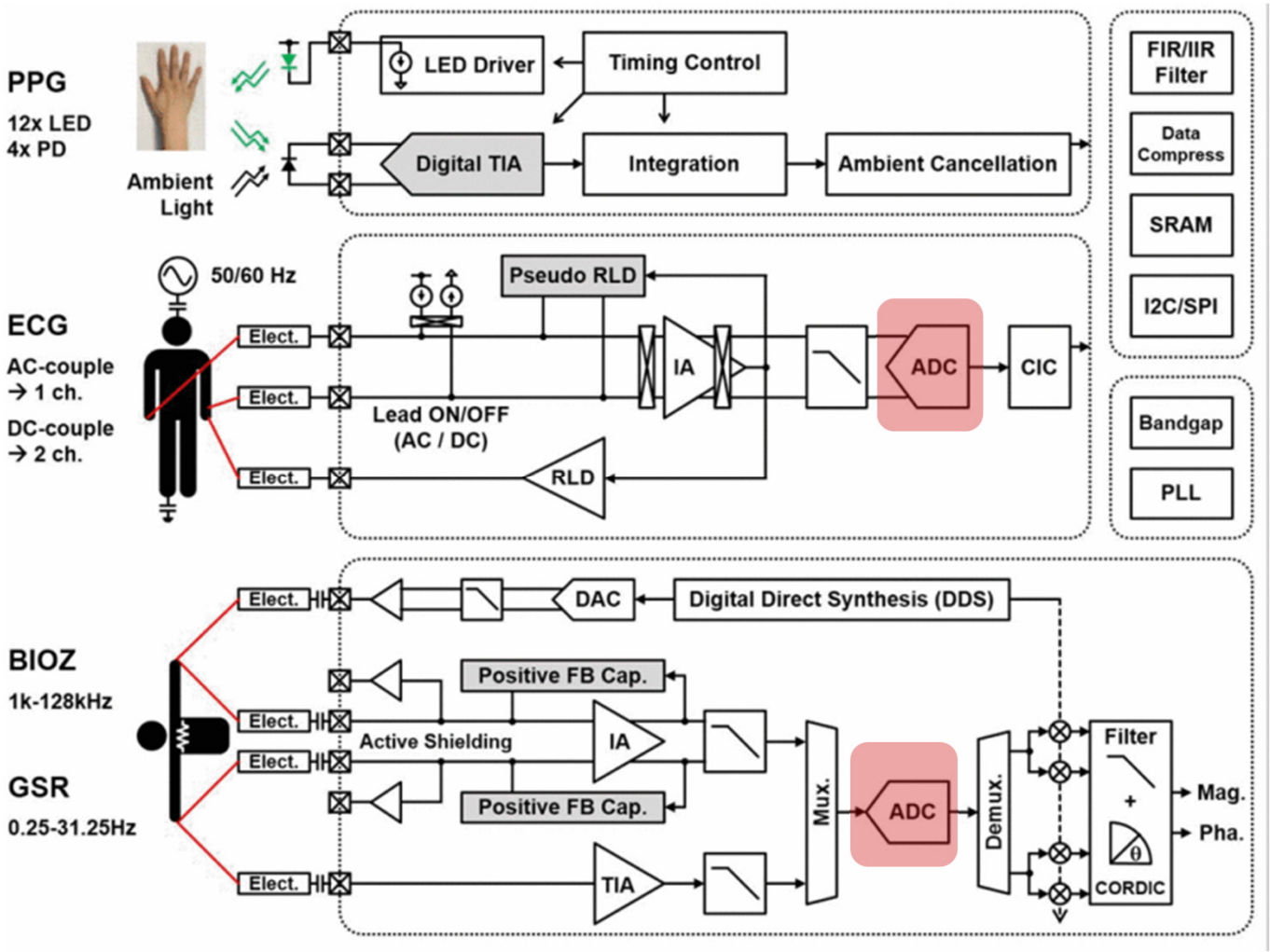
Time-Interleaved ADCs



Application Driver Examples



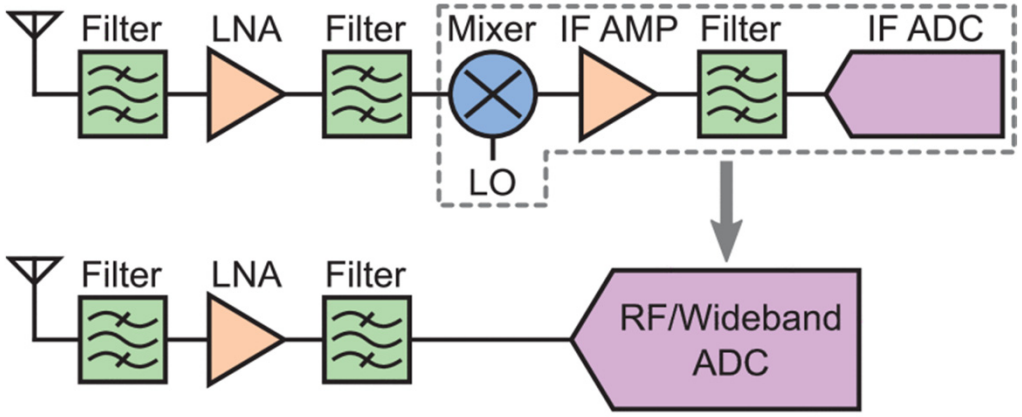
Example: Biosensing SoC for Wearables



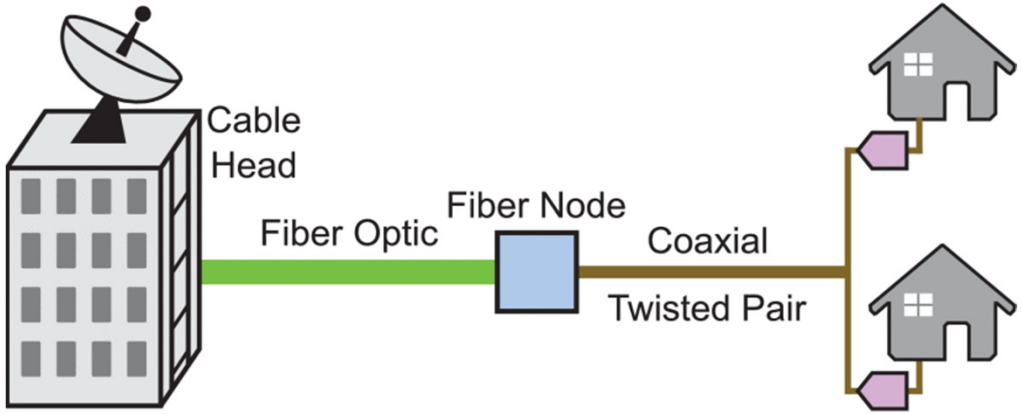
- Low to moderate speed
- Wide range of SNDR
- Low power is key

[Shu, ISSCC 2020]

Example: 5G RF and "Coax" ADCs

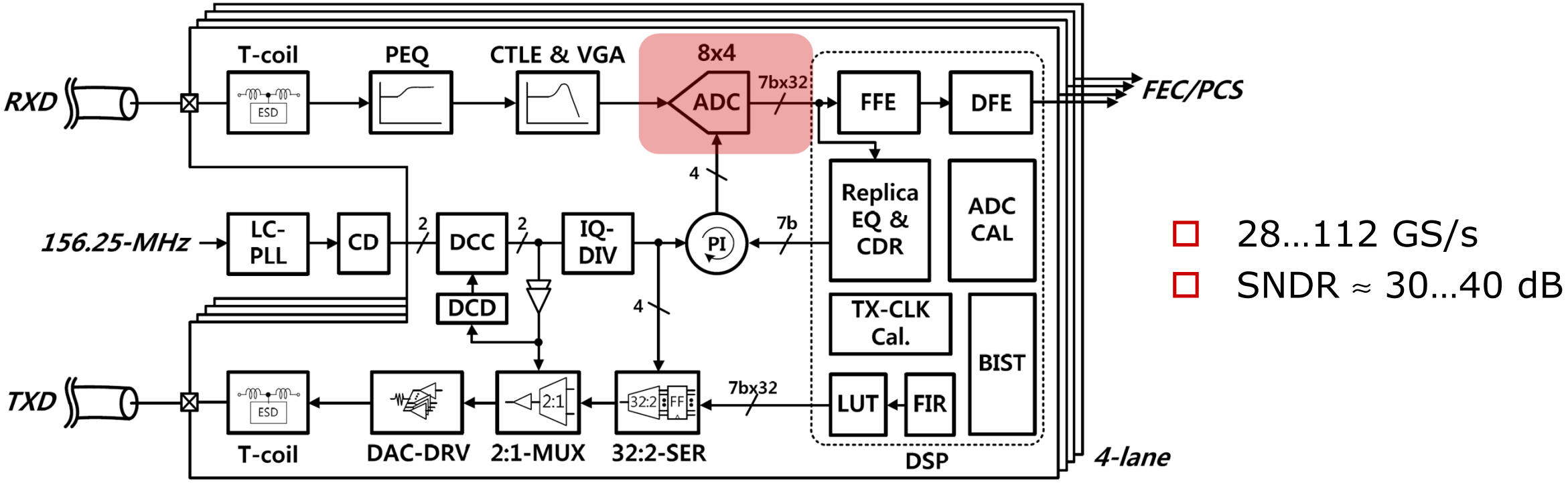


- 1-10 GS/s
- SNDR > 50…60 dB



[Ramkaj, ISSCC 2019]

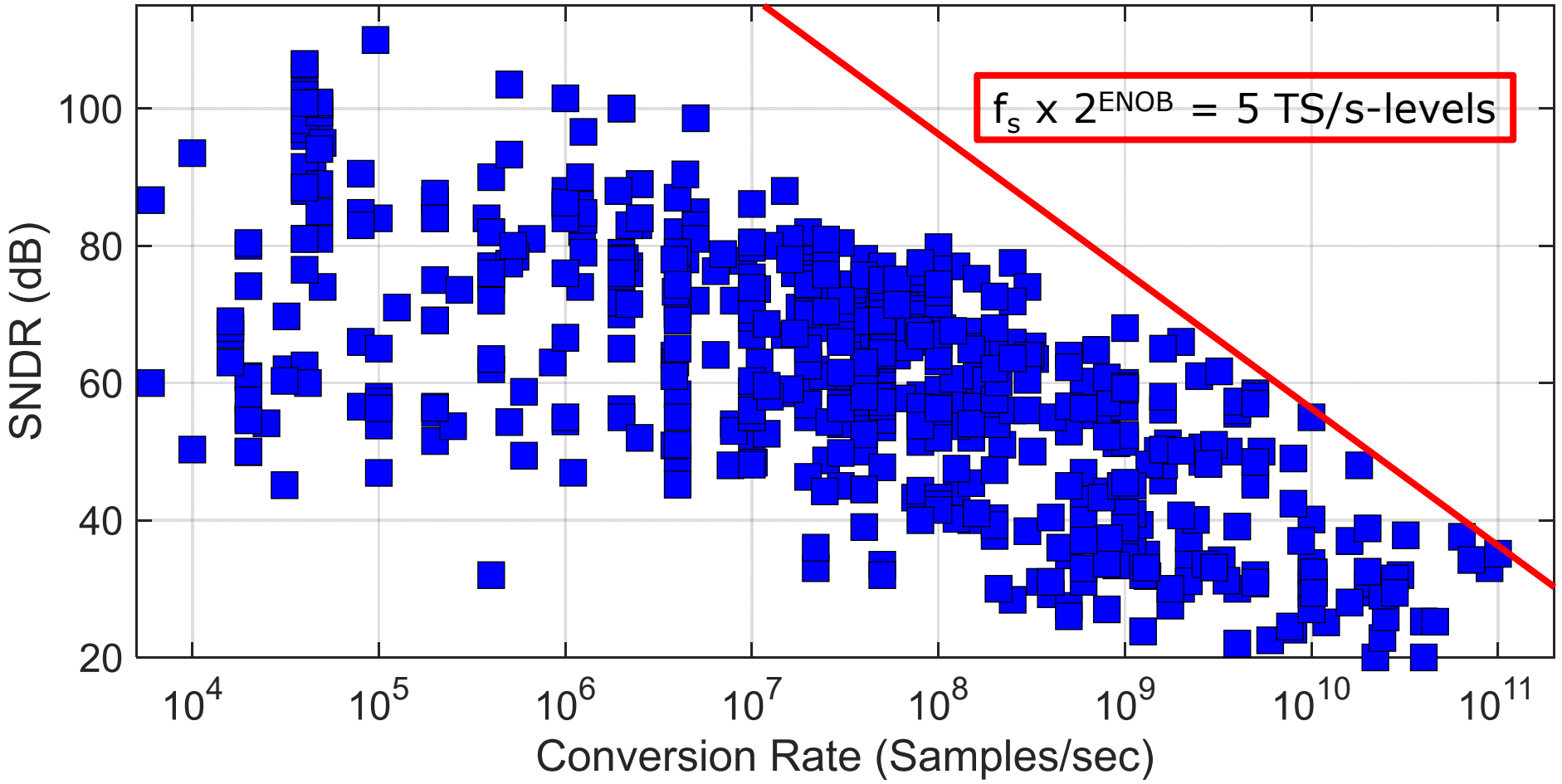
Example: ADC-Based Wireline Transceiver



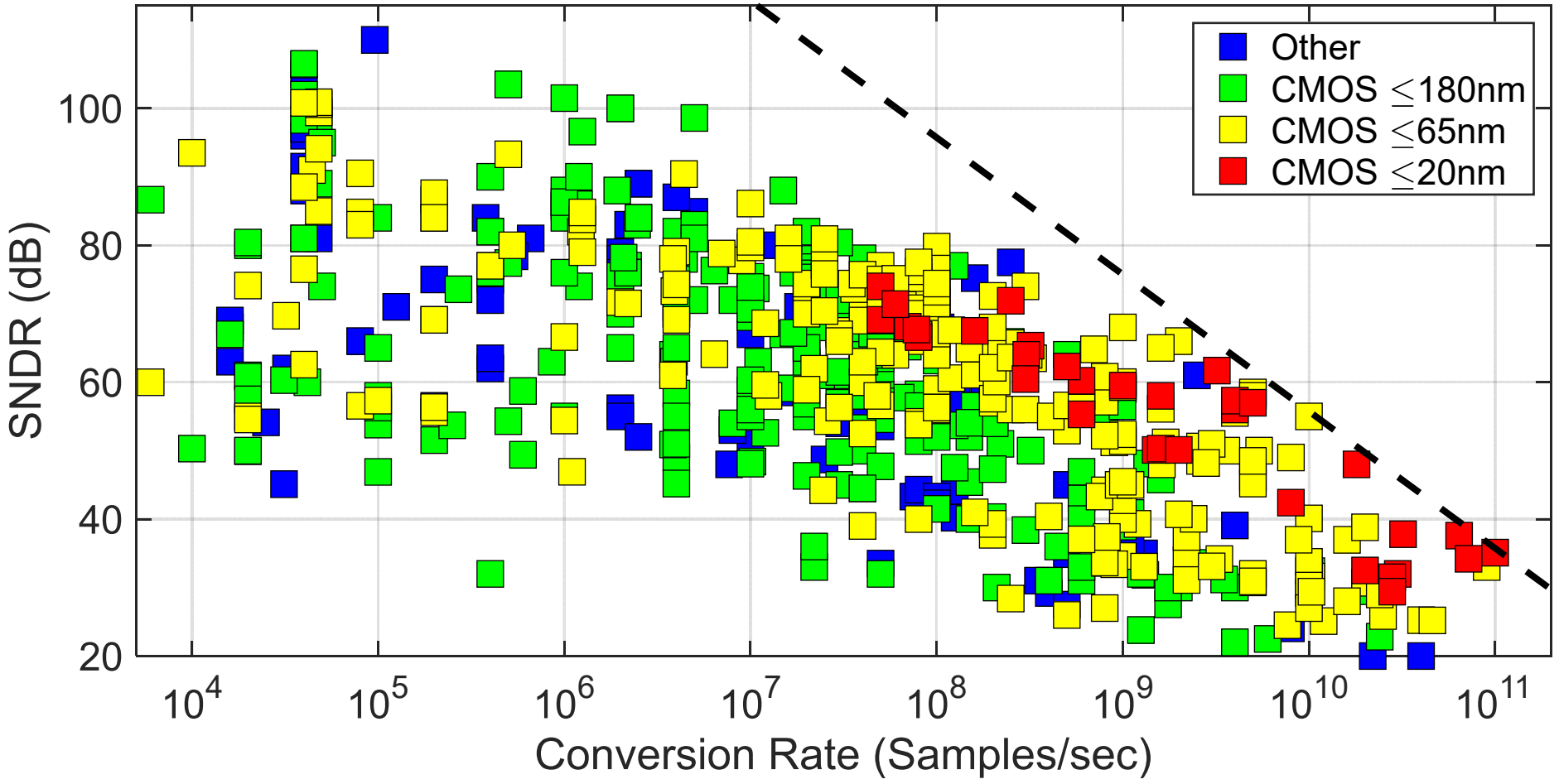
- 28…112 GS/s
- SNDR ≈ 30…40 dB

[Yoo, ISSCC 2020]

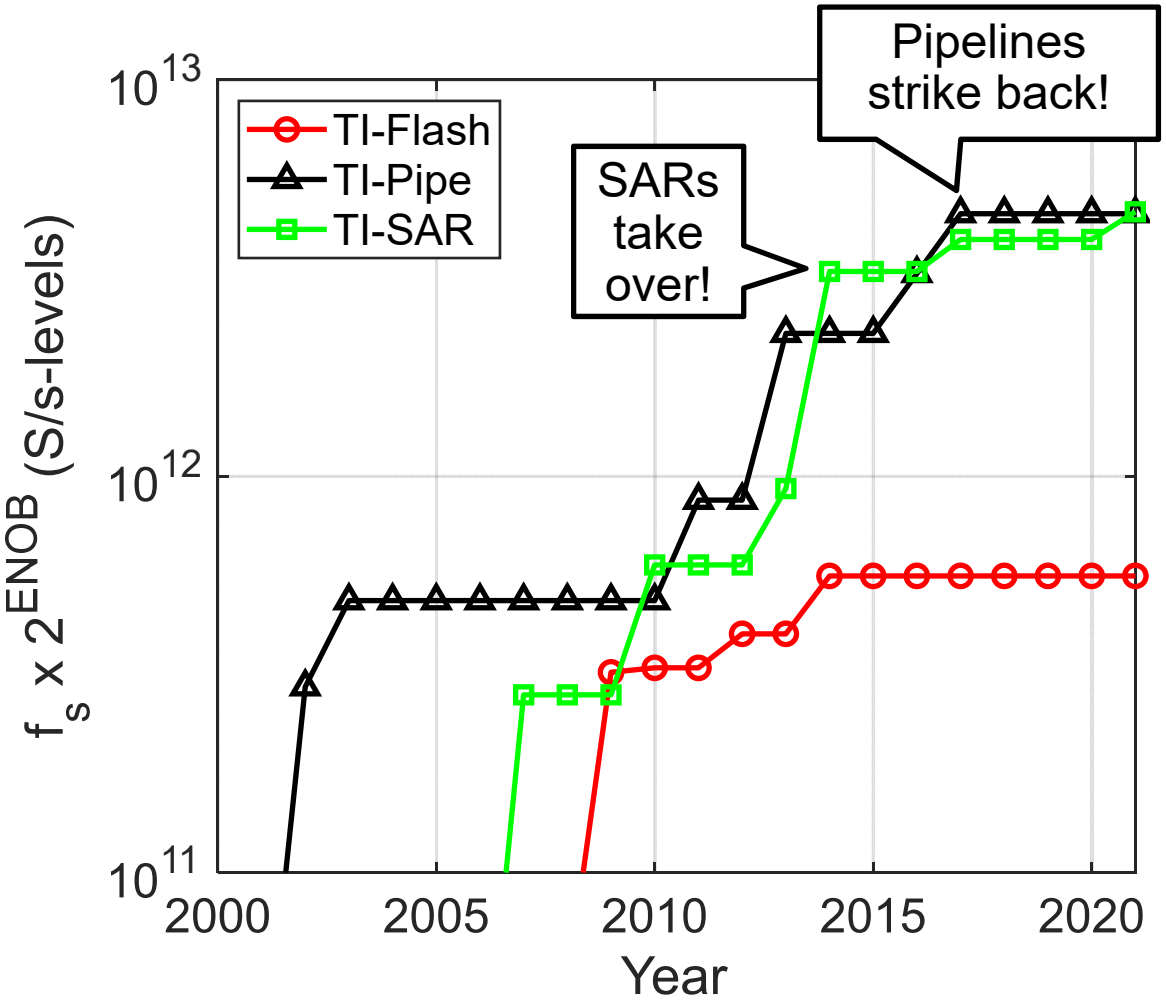
Speed-Resolution Frontier



Speed-Resolution & Process Node



Speed-Resolution Product over Time

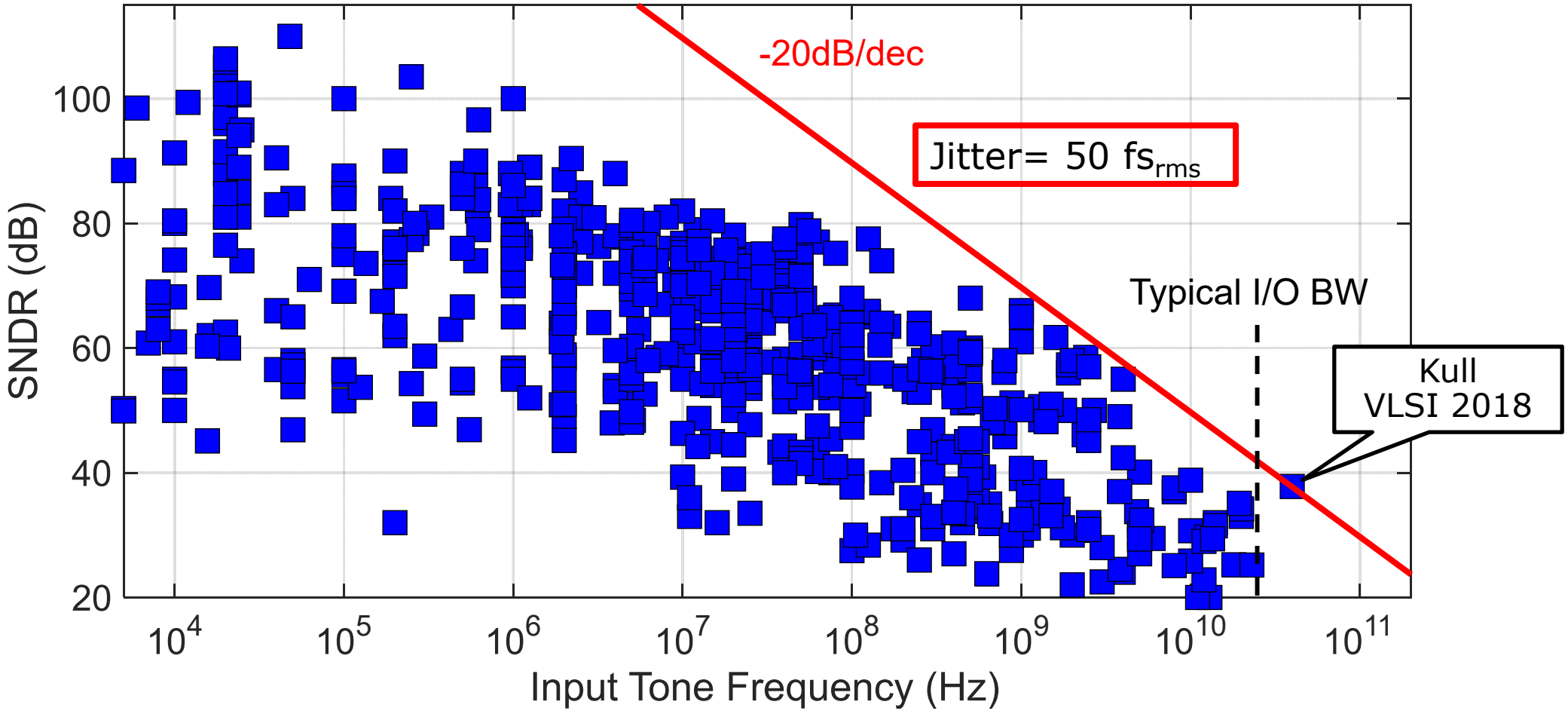


- See also [Murmann, 2016]
- Step-like progress driven by application needs, investments?

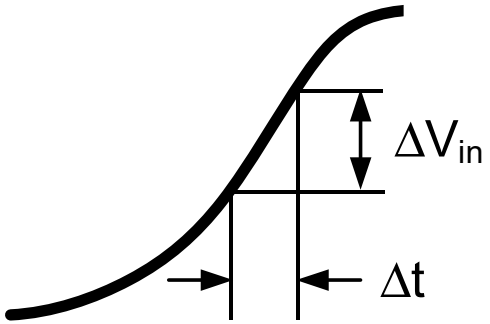
Speed-Resolution Product Limiters

- Highly architecture and application dependent, but often related to
  - Device f_T
  - Input or drive impedance
  - Power constraints
  - Area constraints
  - Cost/ability to absorb output data
  - Input aperture
    - High-speed converters tend to process high-frequency inputs
    - Makes them sensitive to clock jitter
  - Metastability

Input Aperture



Sampling Jitter



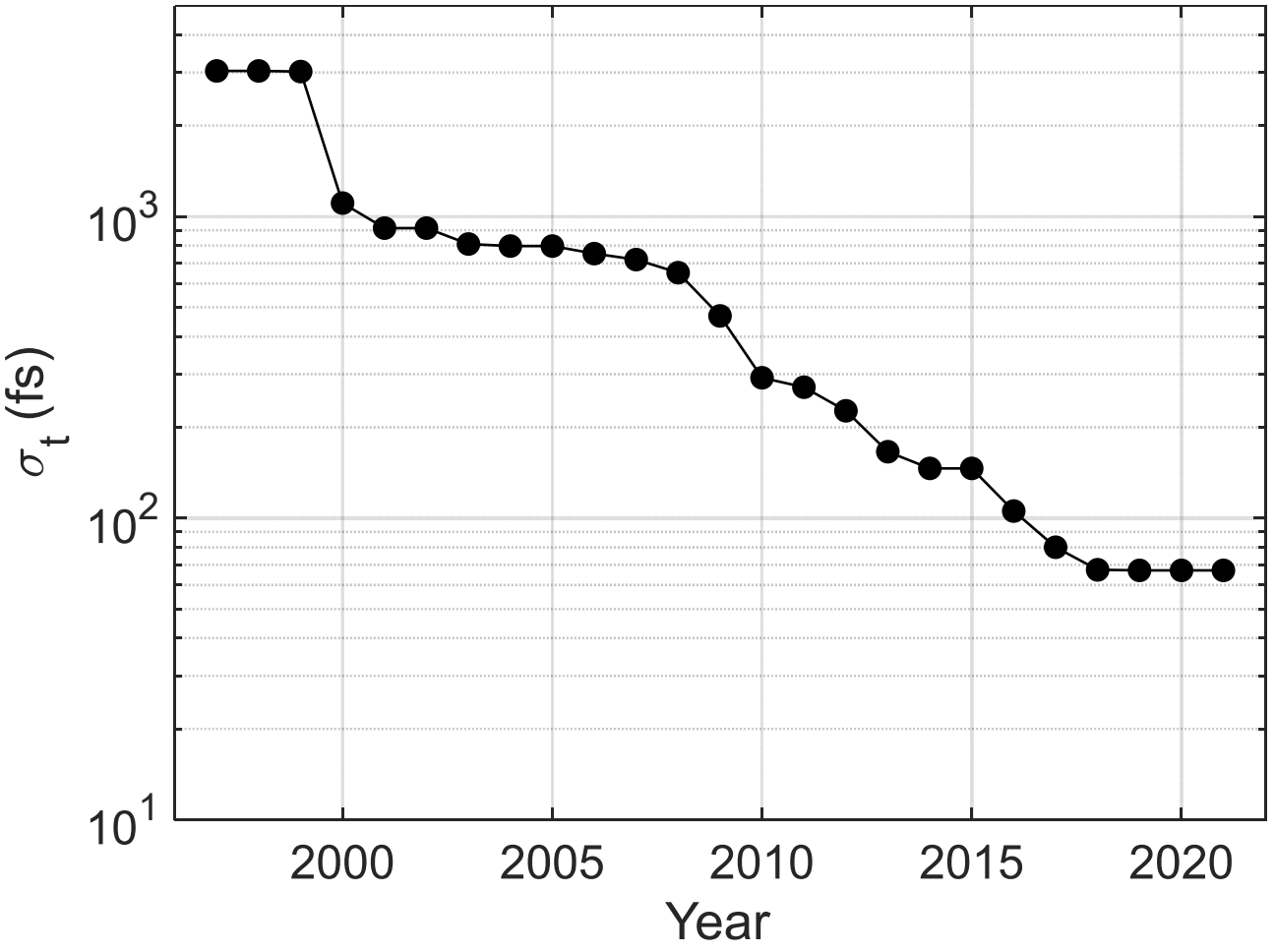
$$\Delta V_{in} \approx \frac{dV_{in}}{dt}\Delta t$$

- SNR limit due to jitter follows from curvature of the signal's autocorrelation function [Da Dalt, 2002]

$$SNR_{jitter} = \frac{1}{\alpha_t \cdot \sigma_t^2} \qquad \alpha_t = -\frac{R''(0)}{R(0)}$$

- Worst case is a single tone at HF (previous slide)
  - In this case $\alpha_t = \omega_{in}^2$
- Wideband or lowpass inputs are less affected
  - Uniform spectrum between $0 \ldots \omega_{in}$ → 4.8dB
  - Wireline channel, 30 dB loss at ω_{in} → ~10dB

Jitter Frontier over Time

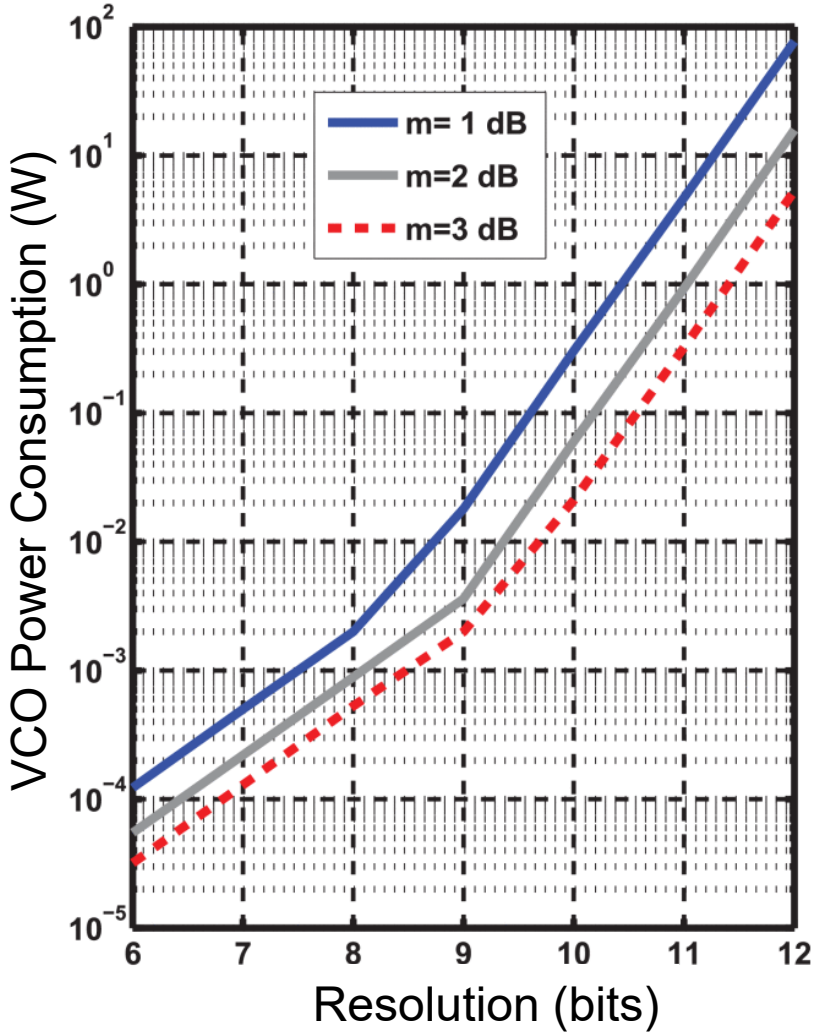


- Plot shows average of three best designs up to respective year
- Input is typically HF sinusoid near $f_s/2$
- Jitter estimated using

$$\sigma_t^2 \approx \frac{1}{\omega_{in,HF}^2 \cdot SNDR_{HF}}$$

- Role of test equipment?

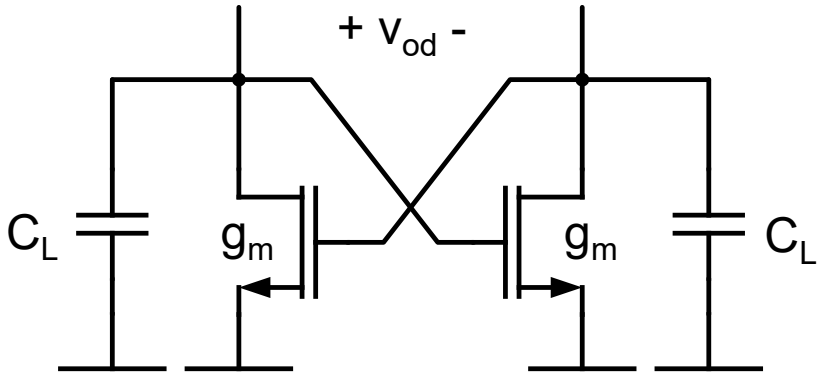
Implications on VCO Power Consumption



- Plots is for a 10 GS/s ADC with m-dB SNR penalty due to jitter
- Input is a sinusoid at Nyquist

[Razavi, 2021]

Metastability

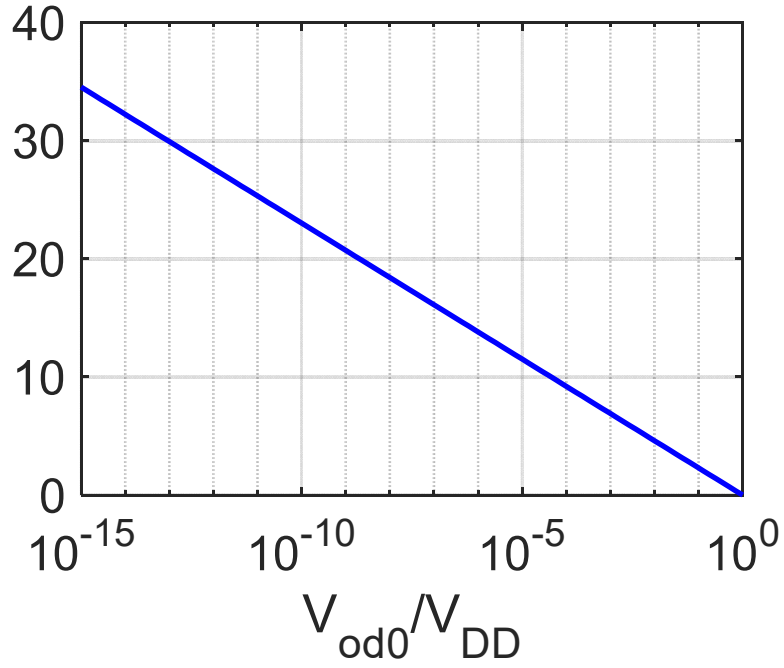


$$\tau \approx \frac{C_{gg} + C_L}{g_m} = \frac{k}{\omega_T}$$

In leading-edge technology:

$$\tau \approx \frac{3}{2\pi \cdot 150GHz} \approx 3ps$$

- Comparators use cross-coupled pairs for fast exponential regeneration
- Small inputs (v_{od0}) lead to long decision times and potential metastability



$$\frac{t_{reg}}{\tau} = -\ln\left(\frac{v_{od0}}{V_{DD}}\right)$$

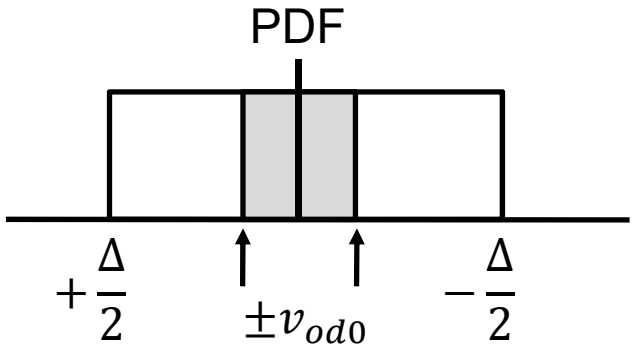
Metastability in a Flash ADC

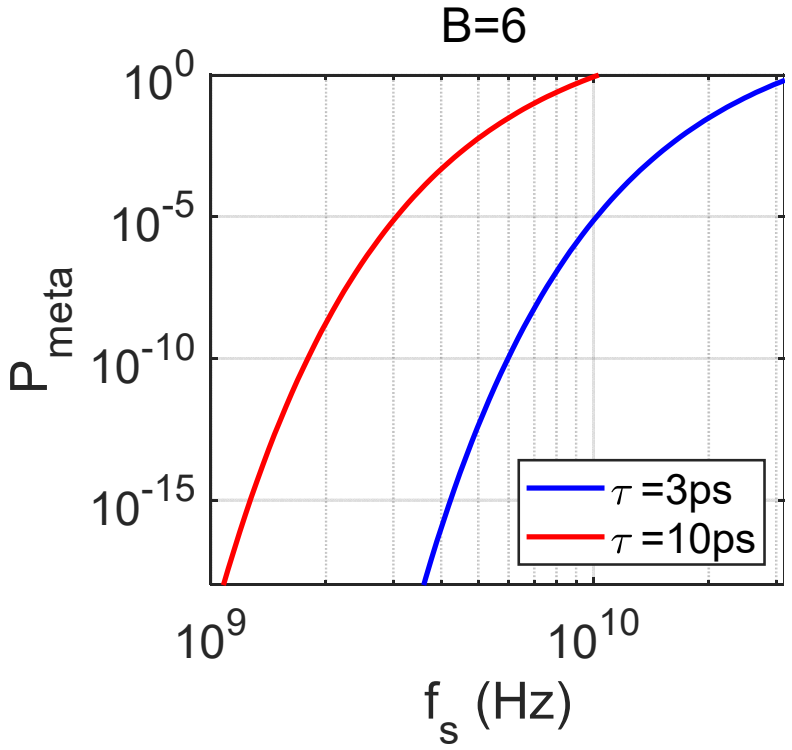
- Smallest input that can be regenerated

$$v_{od0} = \frac{V_{DD}}{e^{T_s/2\tau}}$$

- Probability that a smaller input occurs for comparator at decision boundary

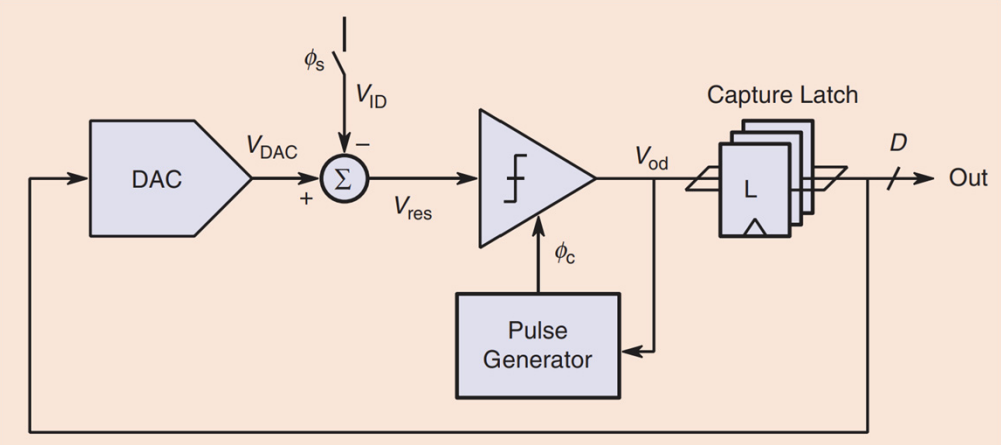
$$P_{meta} = \frac{v_{od0}}{\frac{\Delta}{2}} \approx \frac{v_{od0}}{\frac{1}{2}\frac{V_{DD}}{2^B}} = 2 \cdot 2^B e^{-T_s/2\tau}$$



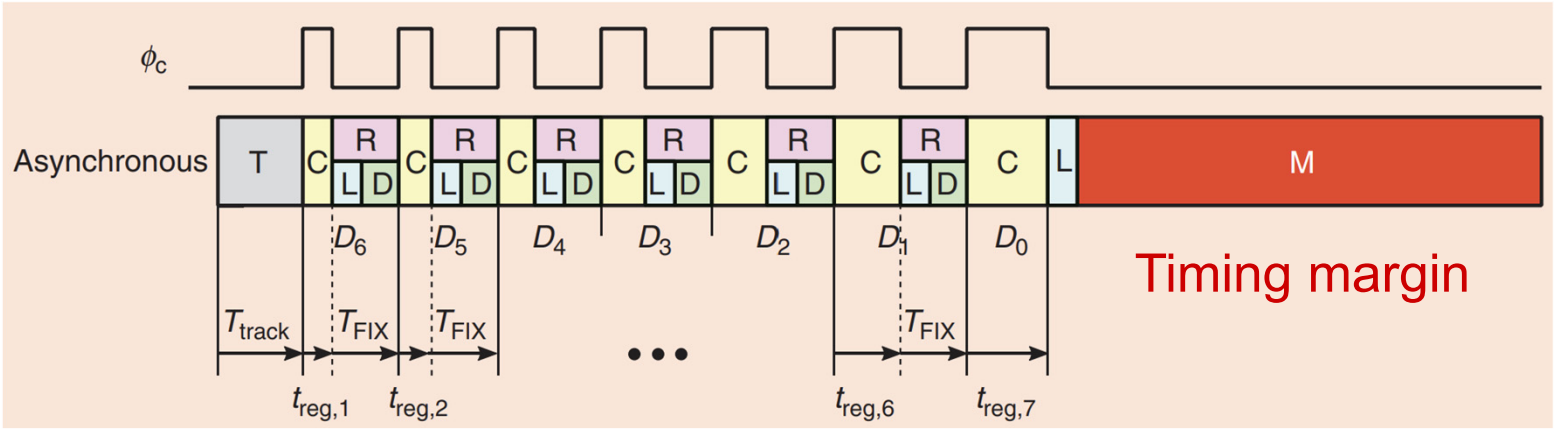


- Difficult to go beyond 10 GS/s
  → Time interleaving

Metastability in an Asynchronous SAR ADC



- Key insight: Need only small timing margin to avoid large metastability errors
- MSBs can borrow time from LSBs
- Error is small when 1-2 LSBs are skipped

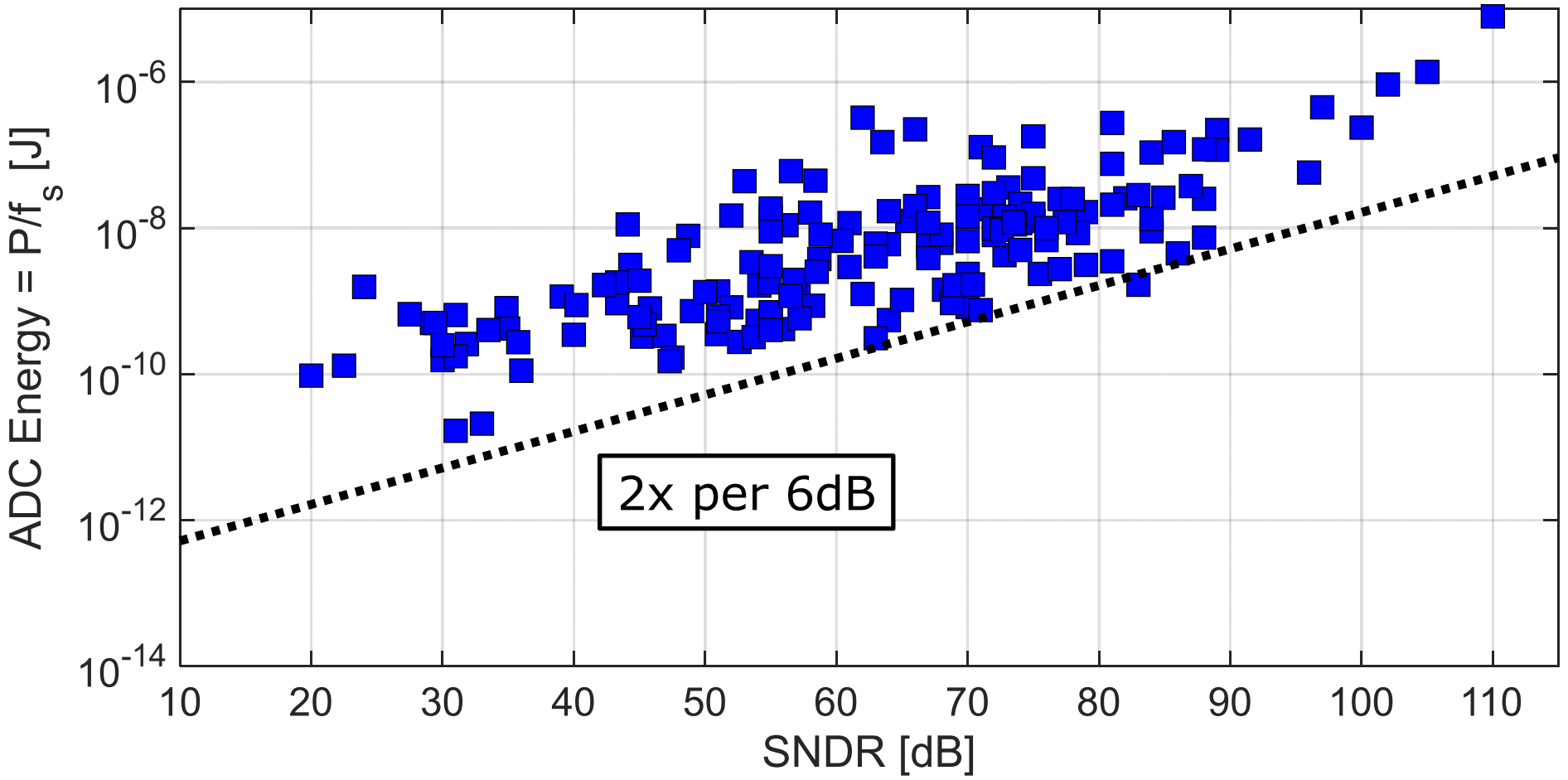


[Yu, 2019]

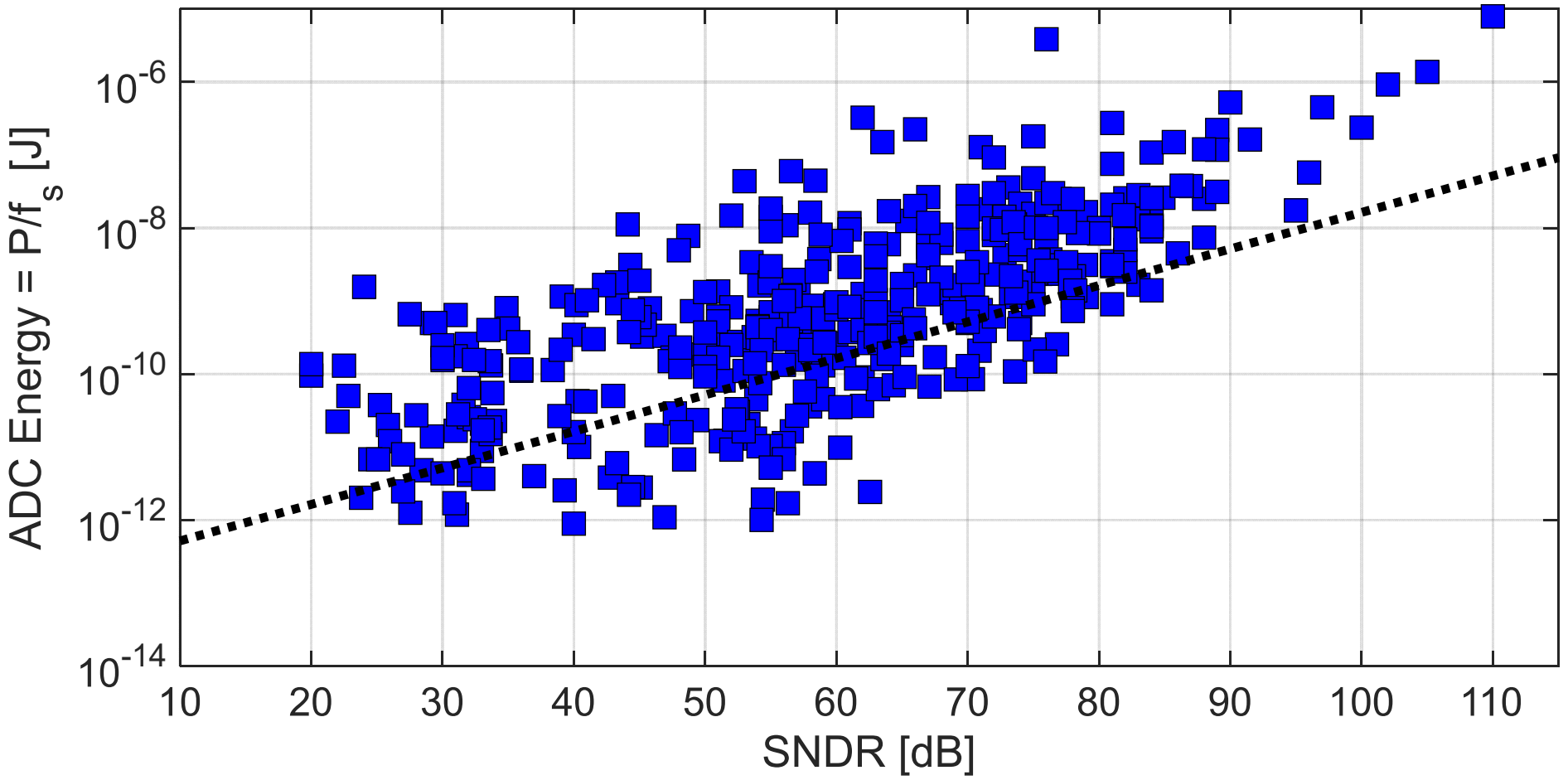
ADC Power Dissipation

- We have so far only looked at conversion rate and resolution, but power dissipation is equally (or often more) important
- To evaluate trends without complex 3D plots, we must agree on first-order dependencies between these metrics
- Straightforward for power and conversion rate
  - Power = Energy/Conversion $\times$ Conversion Rate
- How does Energy/Conversion (P/f_s) scale with resolution (SNDR)?

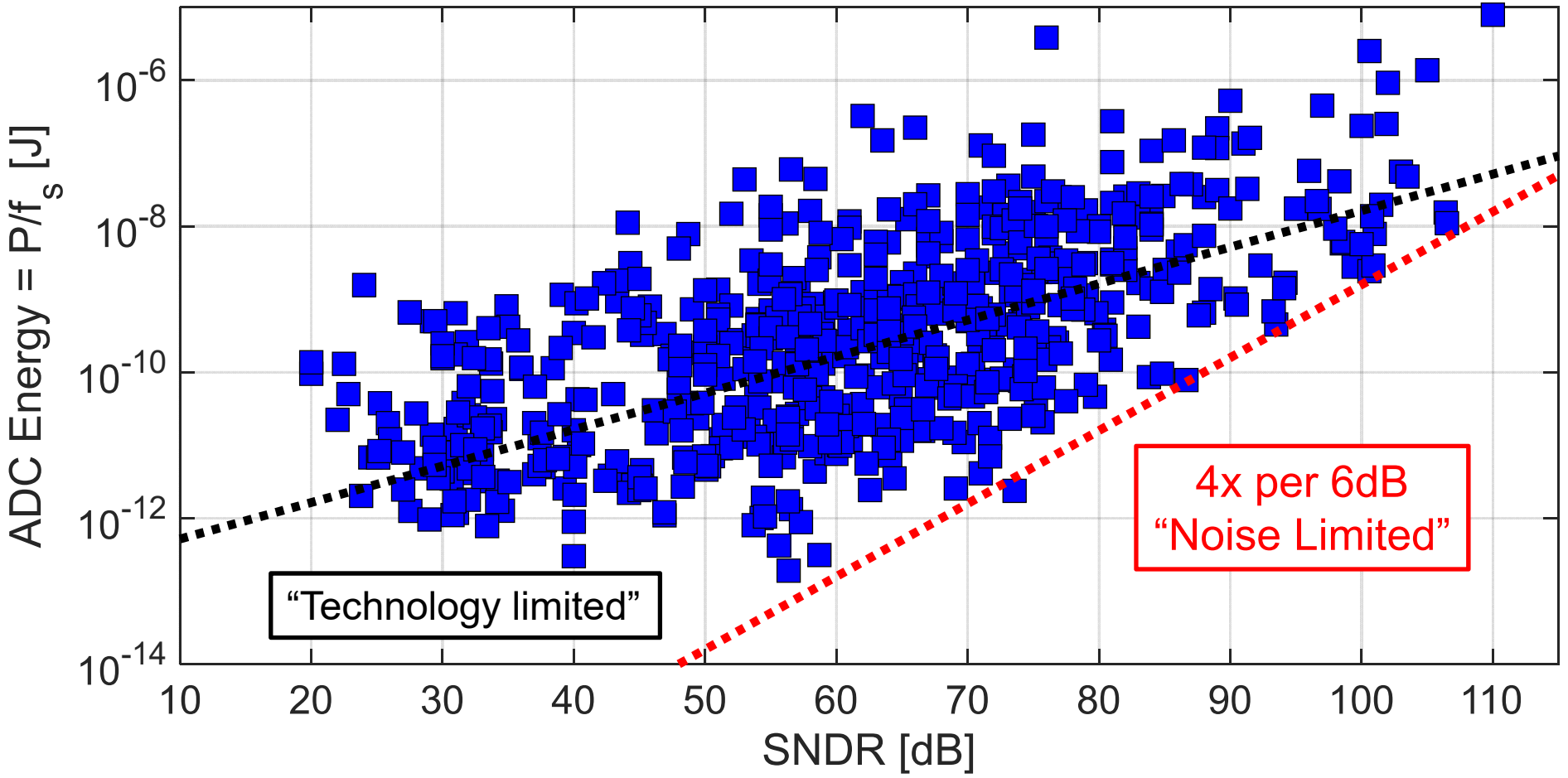
Energy per Conversion (1997-2005)



Energy per Conversion (1997-2013)

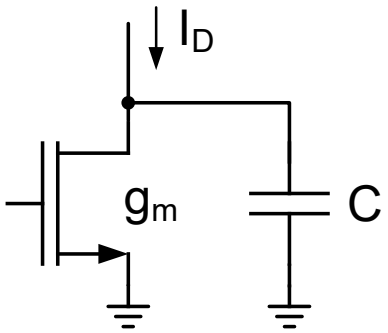


Energy per Conversion (1997-2021)



Trend Toward Noise Limited Designs

- Relentless optimization and technology scaling has resulted in mostly noise-limited designs above SNDR ≈ 50dB
- Resulting slope coincides with tradeoffs in elementary ADC building blocks



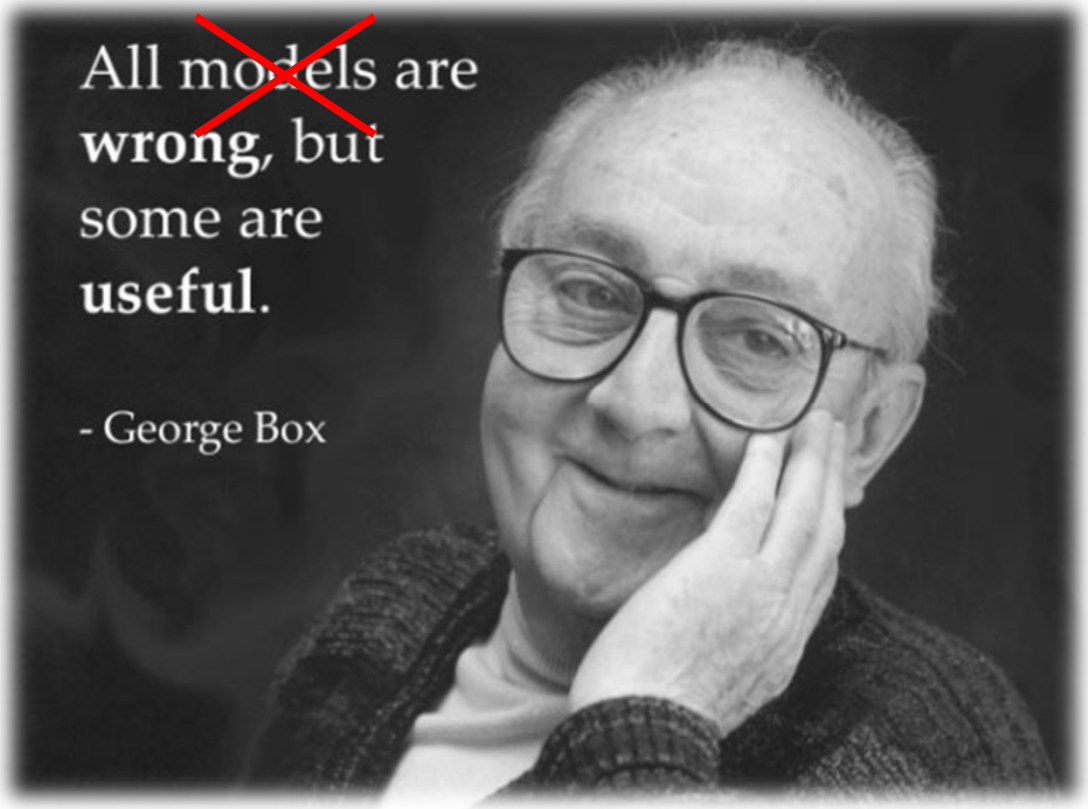
$$SNR \propto \left(\frac{kT}{C}\right)^{-1} \qquad f_s \propto \frac{g_m}{C} \qquad P \propto I_D \propto \frac{g_m}{g_m/I_D} \propto \frac{g_m}{const.}$$

$$\boxed{\frac{P}{f_s} \propto kT \times SNR}$$

Energy increases 4x per 6 dB

ADC Figures of Merit

FoMs



Commonly Used FoMs

- Walden FoM [Walden, 1999]
  - 2x per bit

$$FoM_W = \frac{P}{f_s \cdot 2^{ENOB}}$$

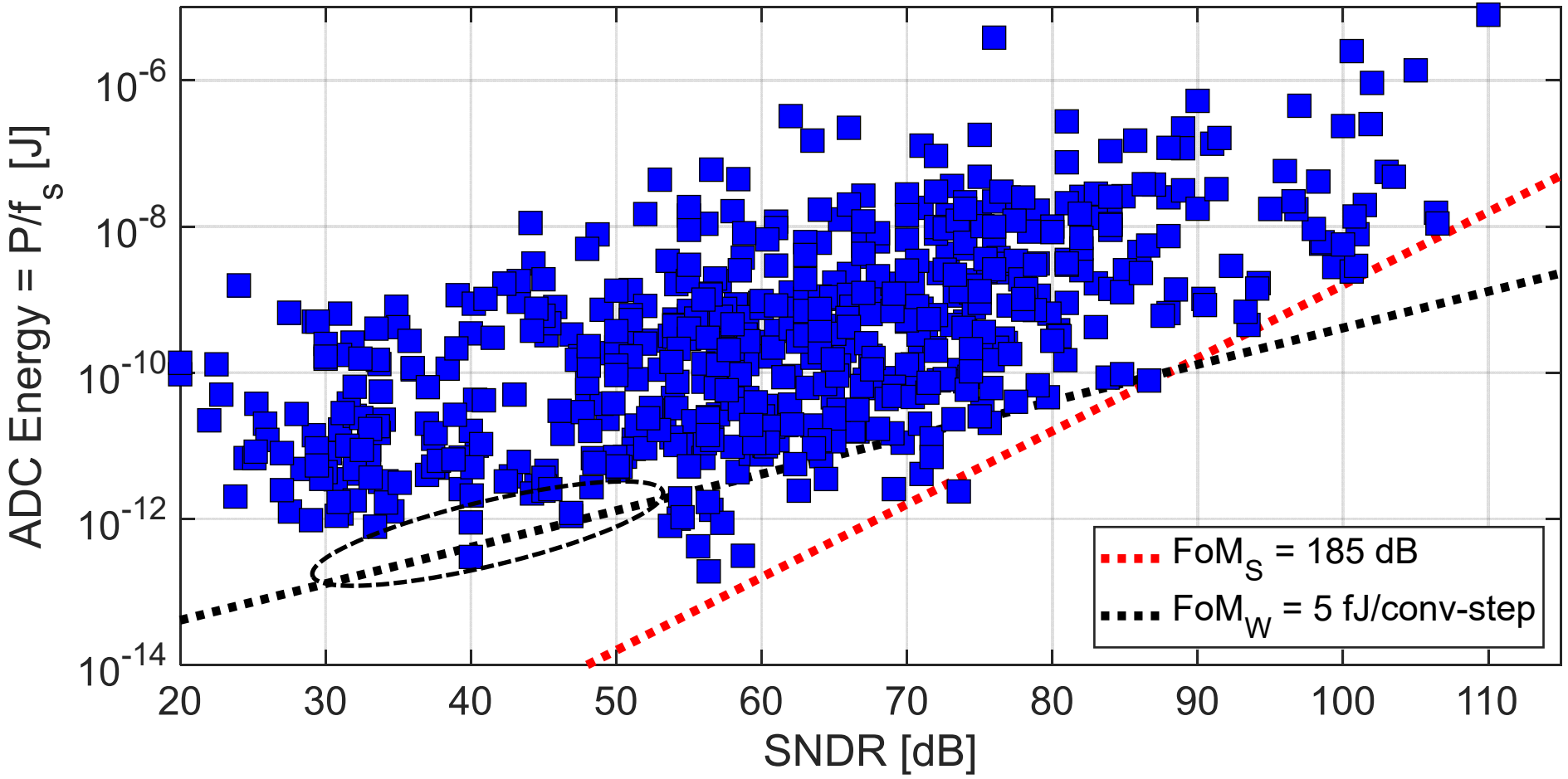
- Schreier FoM (DR) [Schreier, 2005]
  - 4x per bit
  - Ignores distortion

$$FoM_{S,DR} = DR + 10log\left(\frac{BW}{P}\right)$$

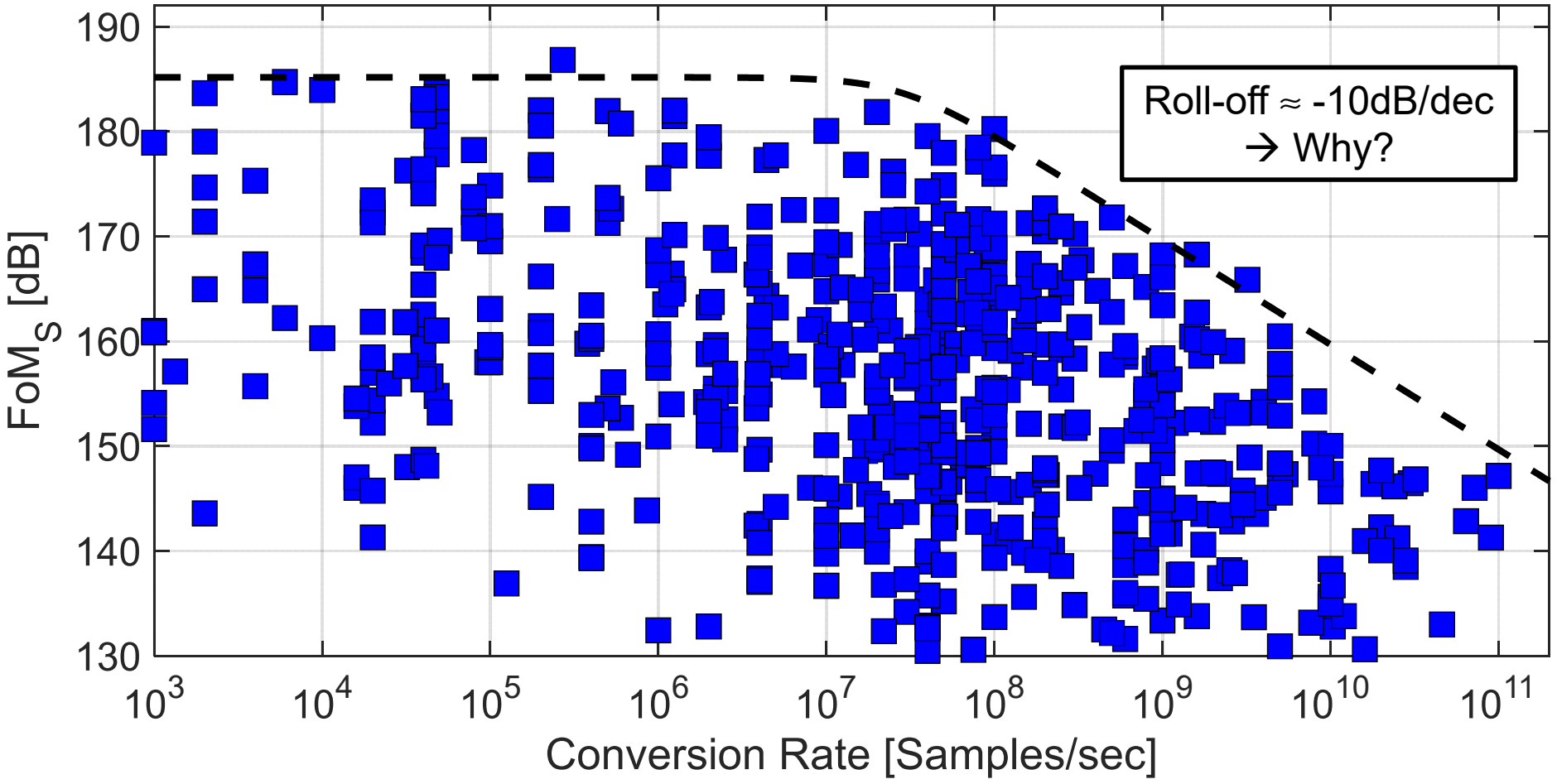
- Schreier FoM (SNDR) [Ali, 2010]
  - 4x per bit
  - Includes distortion
  - Typically use SNDR for near-Nyquist input

$$FoM_S = SNDR + 10log\left(\frac{f_s/2}{P}\right)$$

Example FoM Lines



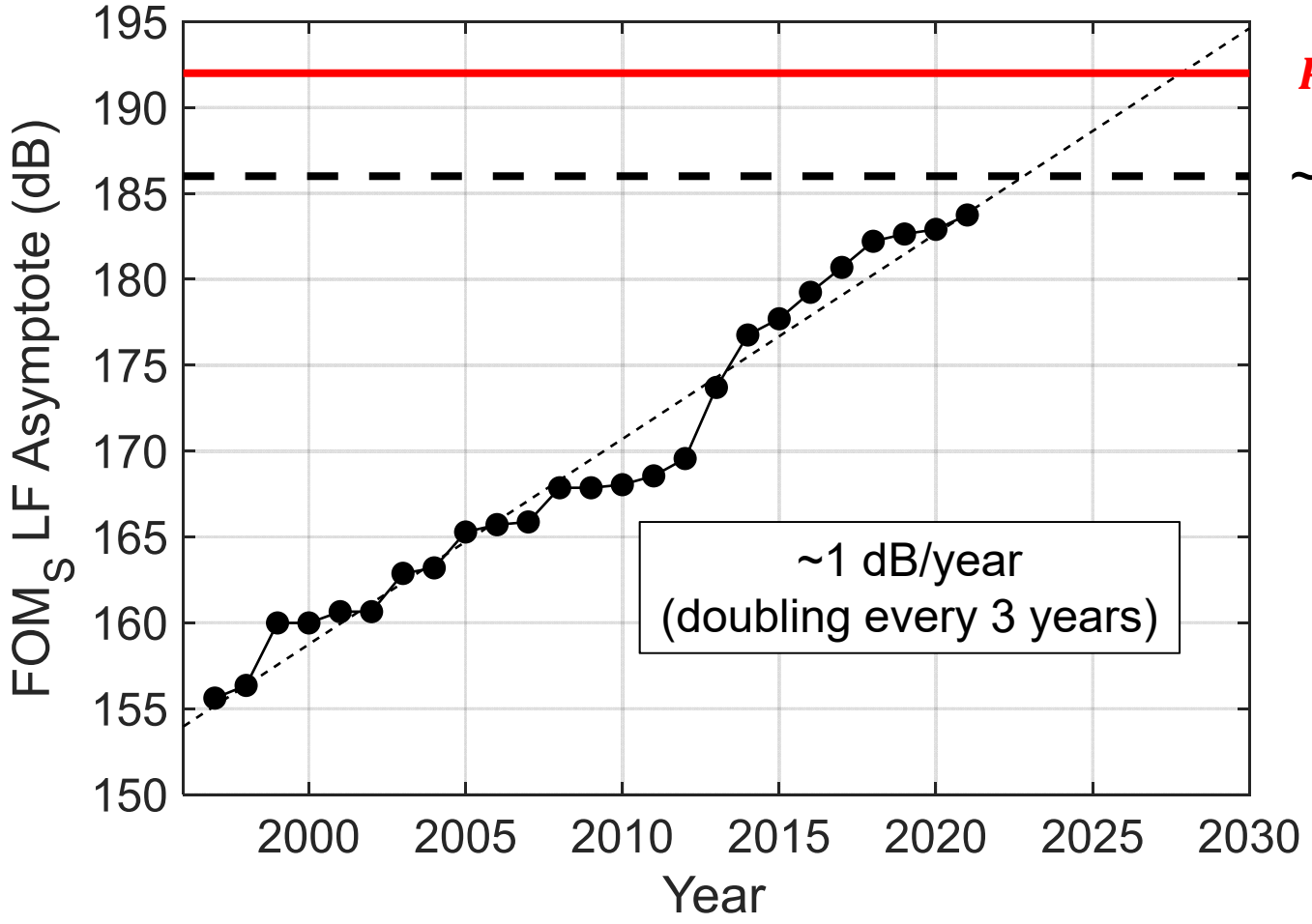
FoM_S vs. Conversion Rate



FoM_S Roll-Off

- Transistors become less efficient at high speed
  - Required transistor $f_T \uparrow \rightarrow g_m/I_D \downarrow$
  - Assumption of linear power scaling with f_s in FoM_S equation falls apart
- Many high-speed designs tend to lie in the "technology limited" region
  - Assumption of 4x power scaling per 6 dB in FoM_S does not apply
- Other factors include overhead due to interleaving, low-jitter clocking, …
- **Generally (independent of FoM choice), limit comparisons to designs with similar speeds and resolution!**

Low-Frequency FoM_S over Time

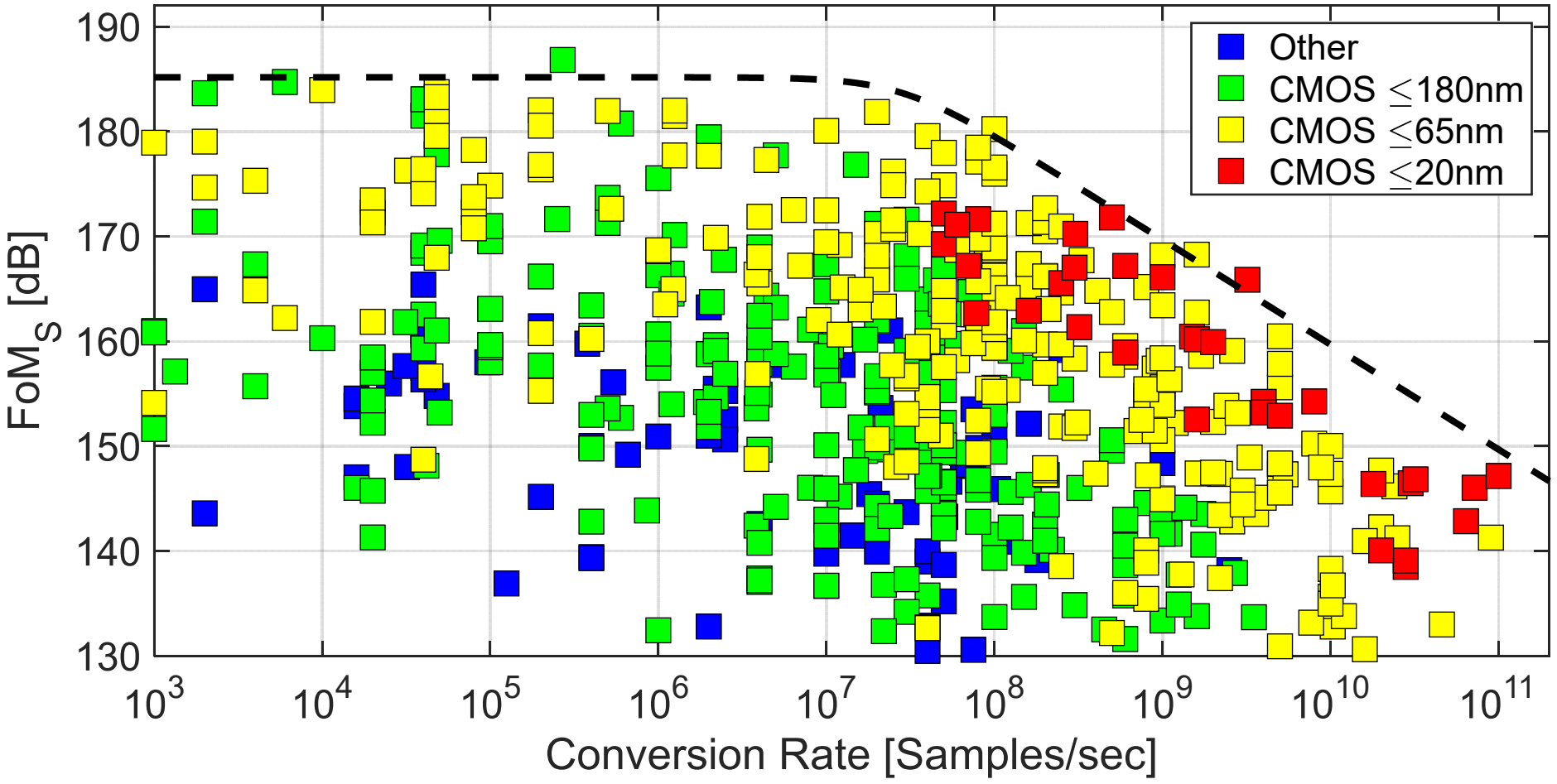


$P/f_s = 8kT \times SNR$

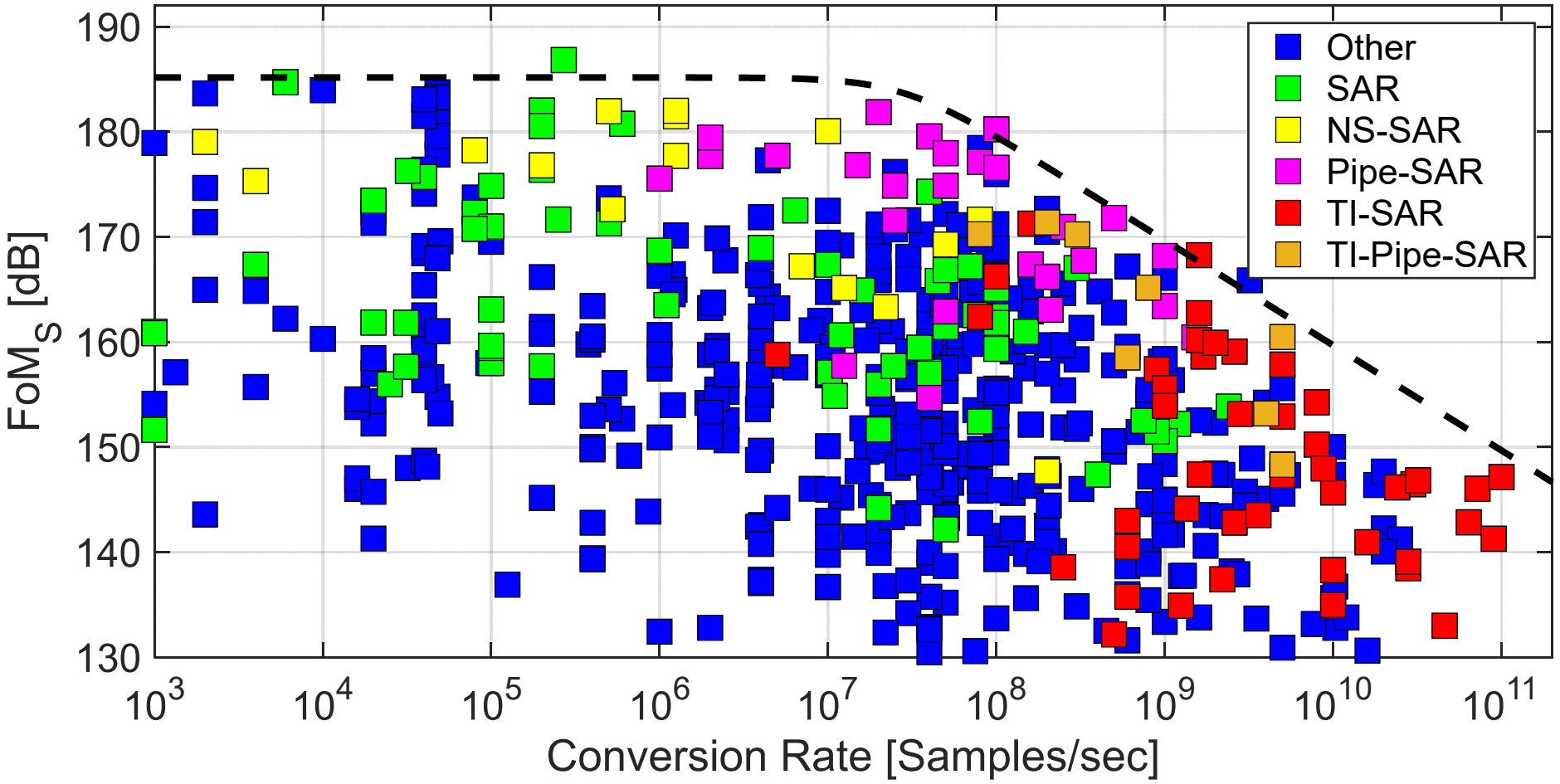
~Practical limit (?)

- 8kT×SNR limit corresponds to rail-to-rail class-B circuits [Vittoz, 1990]
- Difficult to surpass!

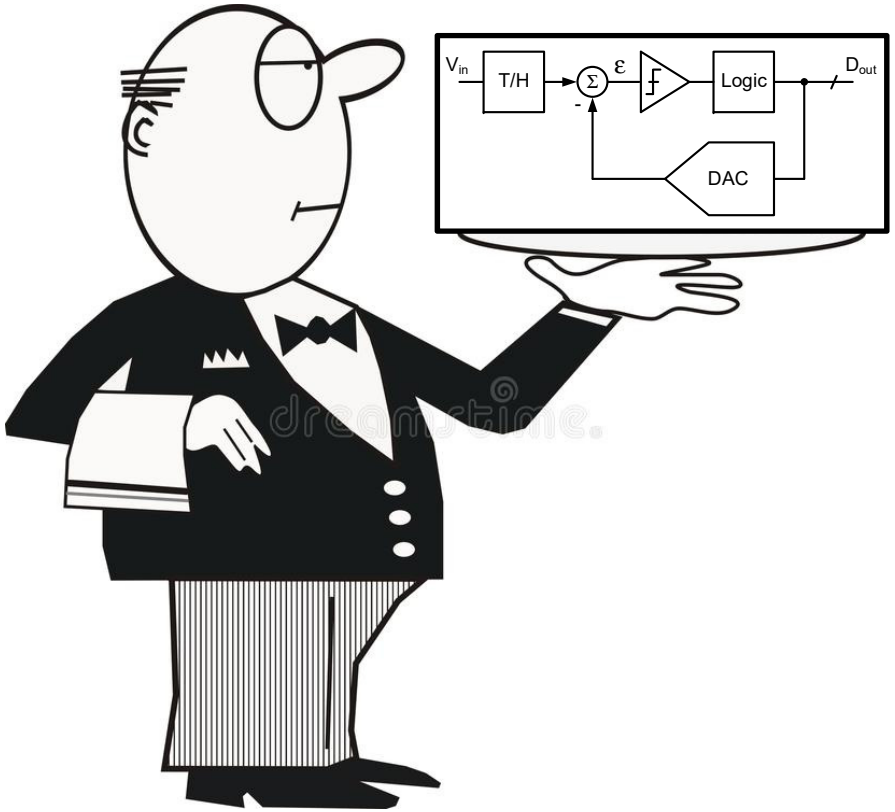
FoM_S vs. Conversion Rate & Process Node



FoM_S for SAR-Based Converters



How Do You Like Your SAR ADCs Served?



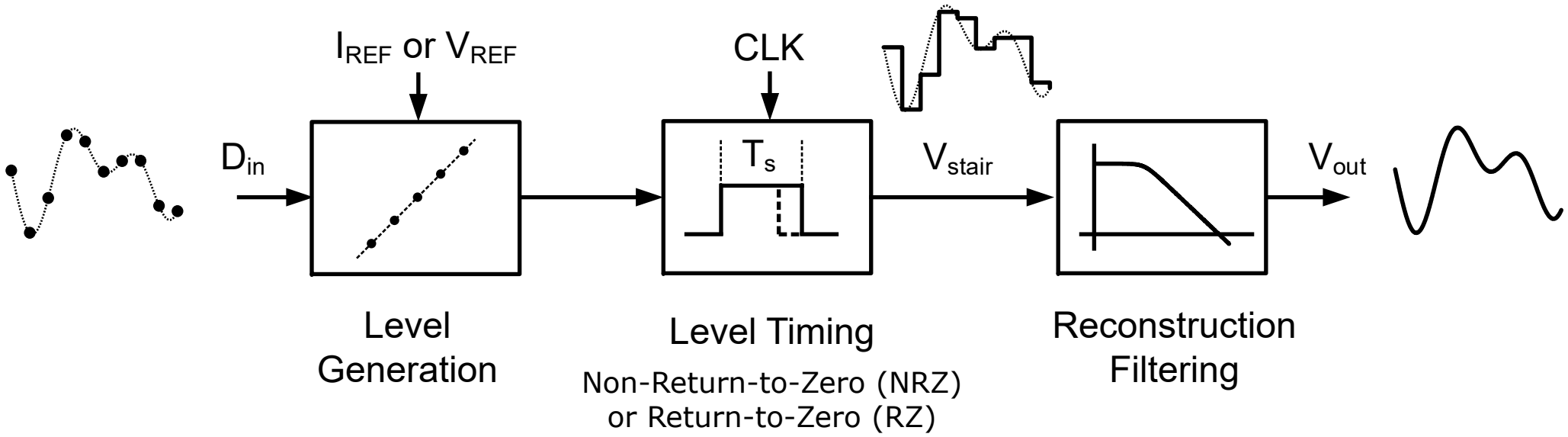
- Plain?
- Noise-shaped?
- Pipelined?
- Interleaved?
- Pipelined & interleaved?

Outline

- ADCs
  - Metrics
  - Architectures
  - Speed, resolution, energy tradeoffs and trends
  - Building block considerations
  - Application aspects

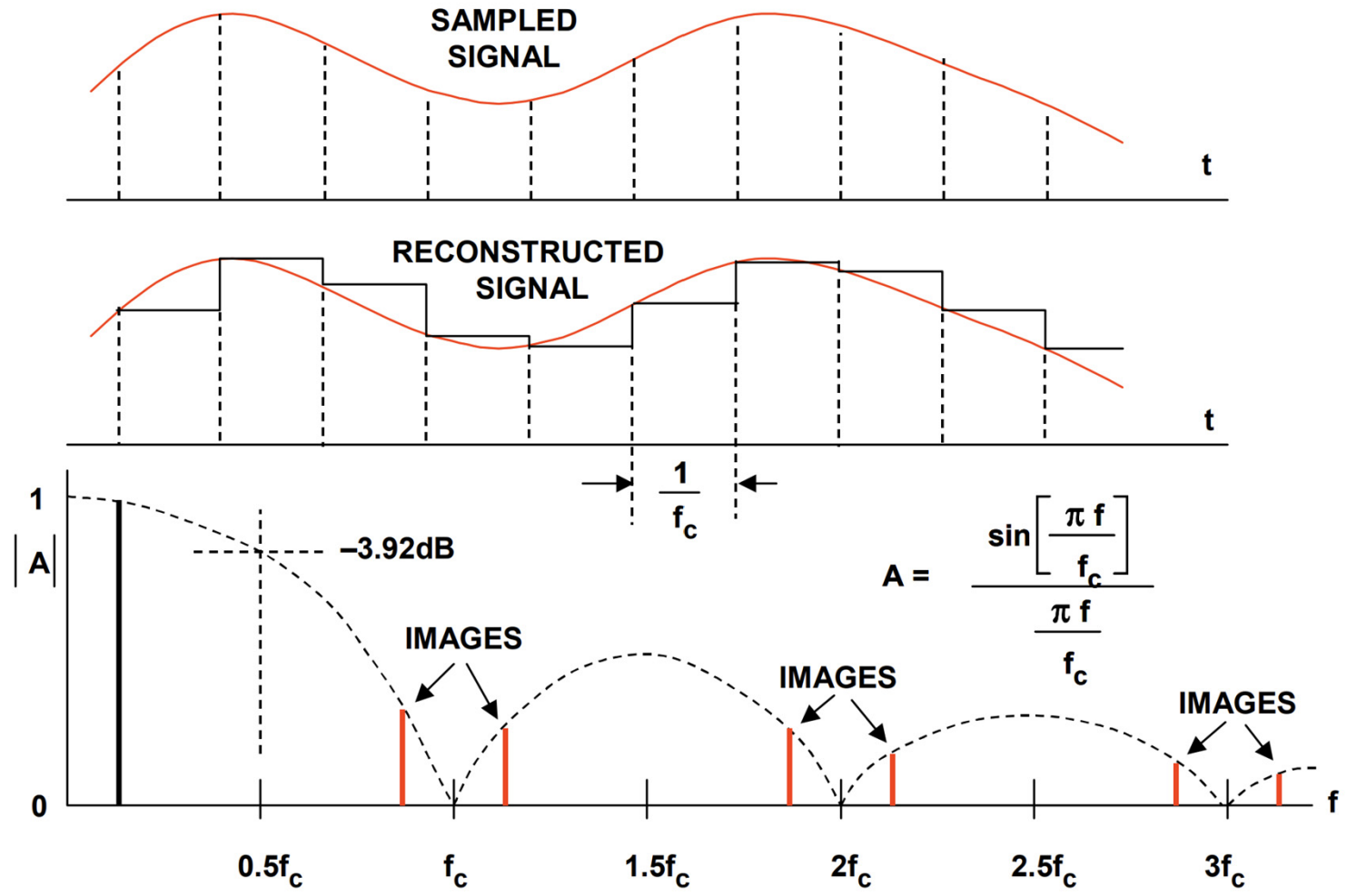
- DACs
  - Output spectrum & metrics
  - Introduction to current steering
  - Timing and jitter requirements
  - Performance trends
  - Application aspects

Conceptual View of a Nyquist D/A Interface



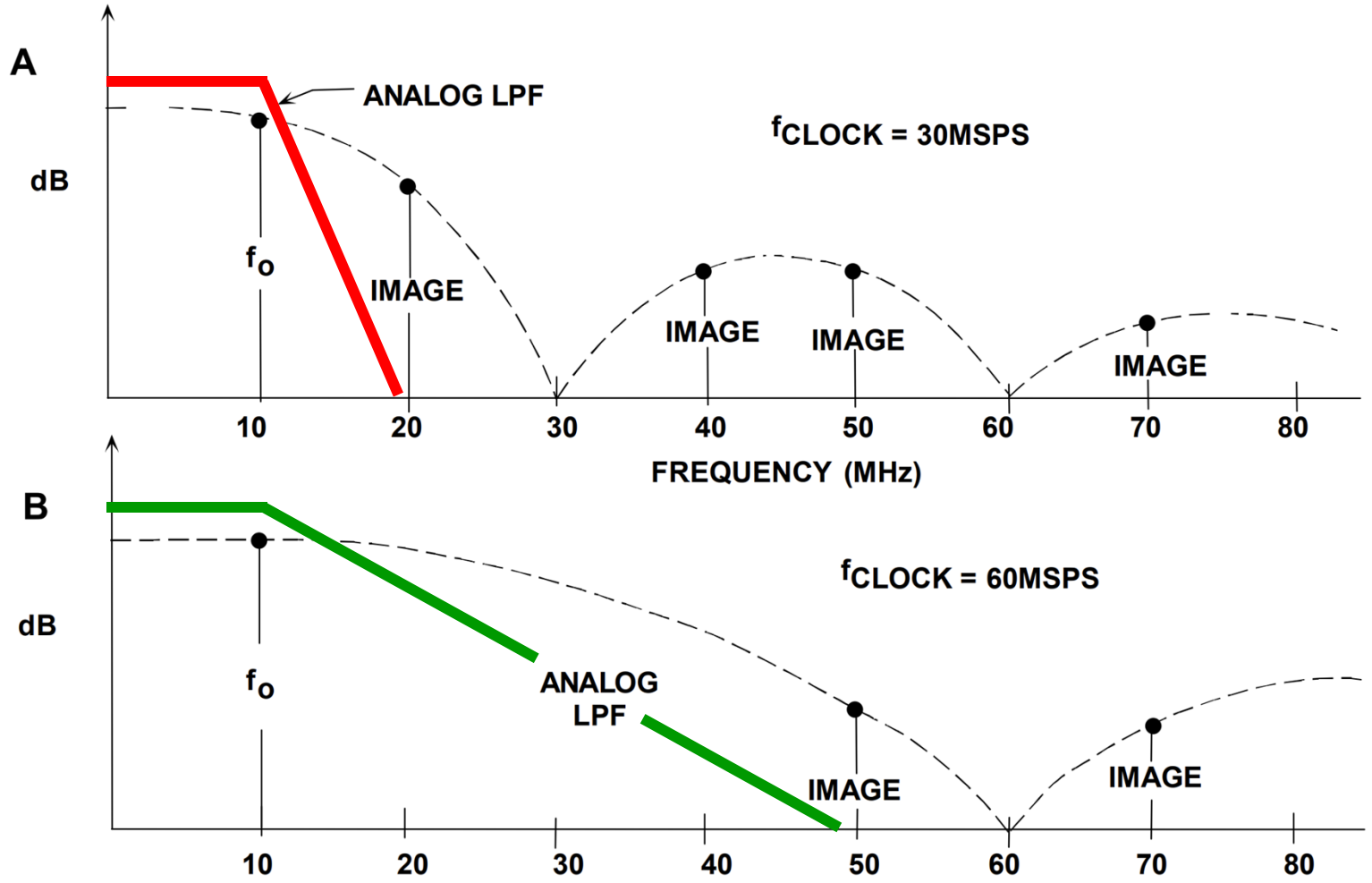
- Two challenges
  - Accurate mapping of digital input to analog levels
  - Accurate timing of level transitions

Spectral Images For NRZ Output



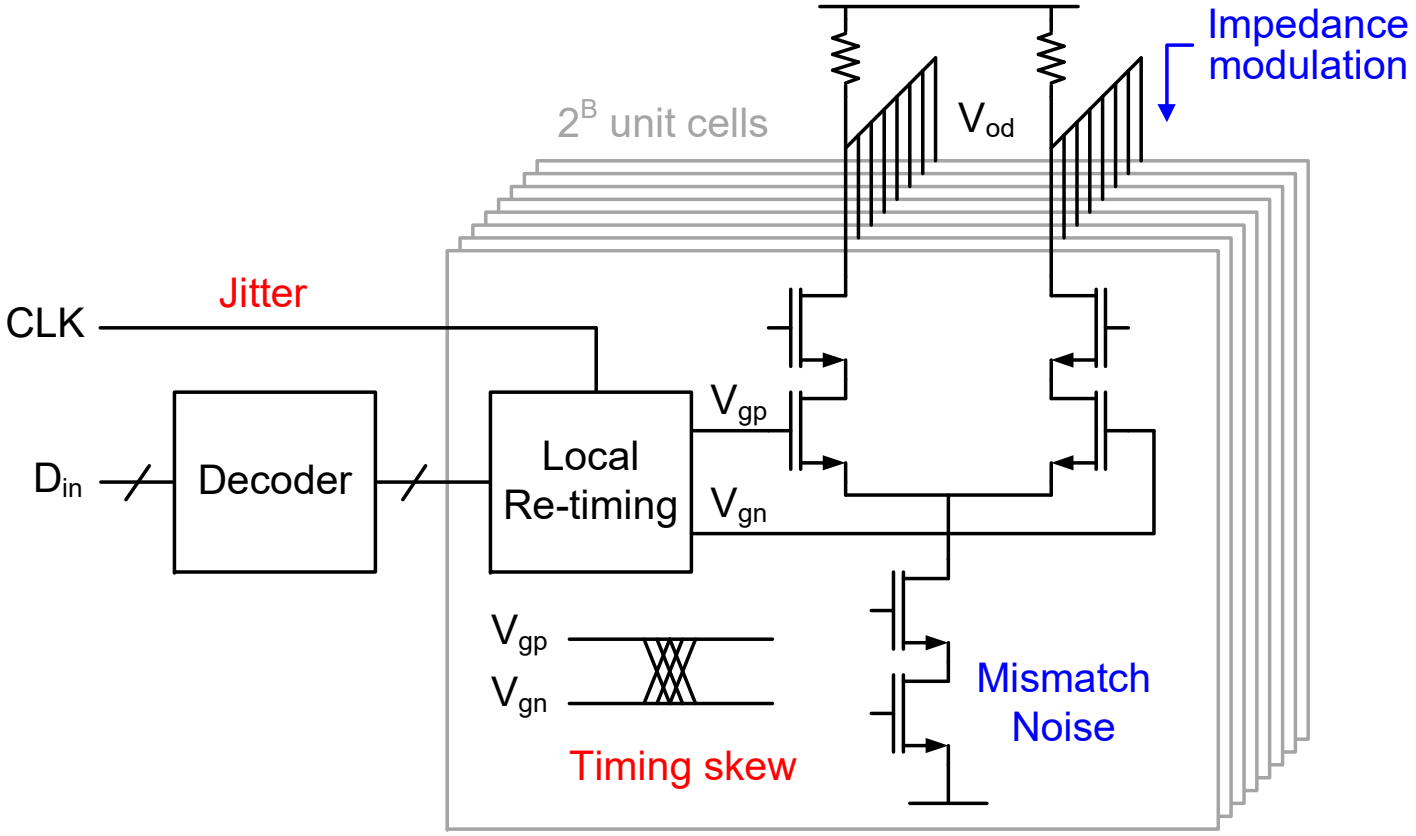
[Kester, 2005]

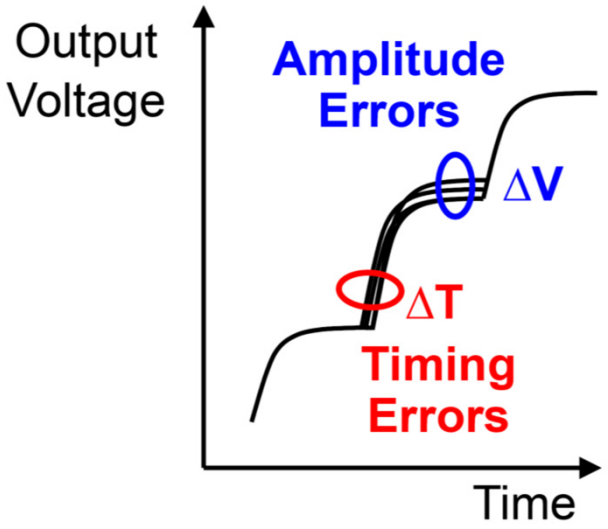
Oversampling Reduces Filter Requirements



[Kester, 2005]

Current Steering Architecture



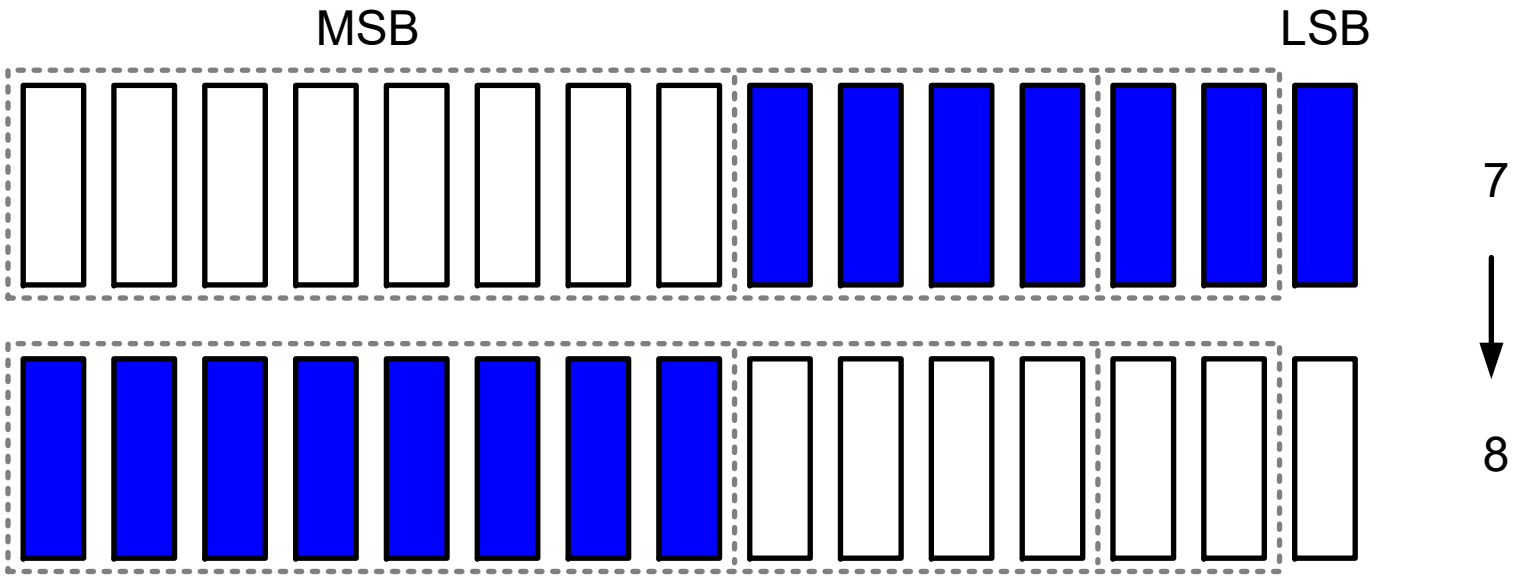


[Lin, ISSCC 2018]

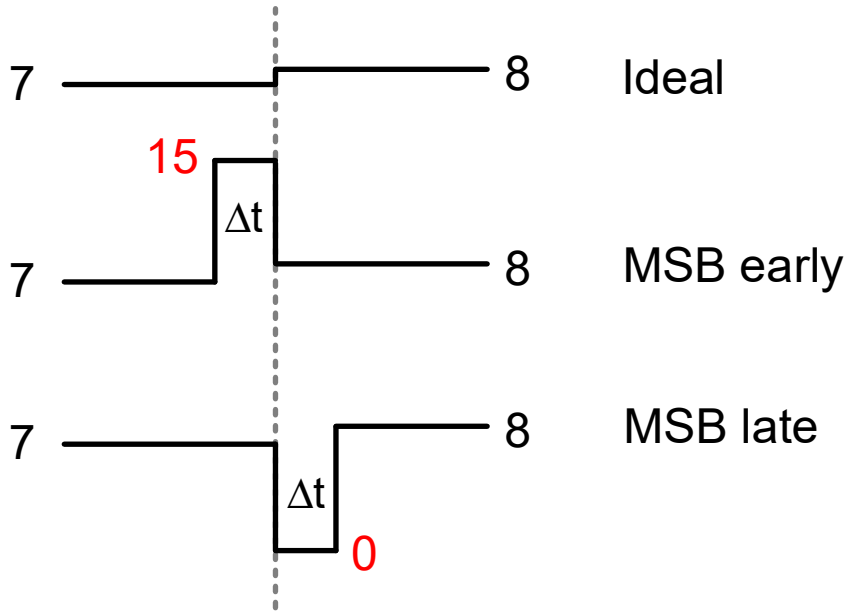
- Unit cell grouping has significant effect on achievable performance

Binary Grouping

- No decoder needed, but MSB transition is a major issue
- Consider 4-bit example below
  - Turn off 7, turn on 8 to go from 7 to 8
  - Both amplitude and timing errors are a significant problem



Timing Glitch for Binary Grouping



For single-tone input, can show

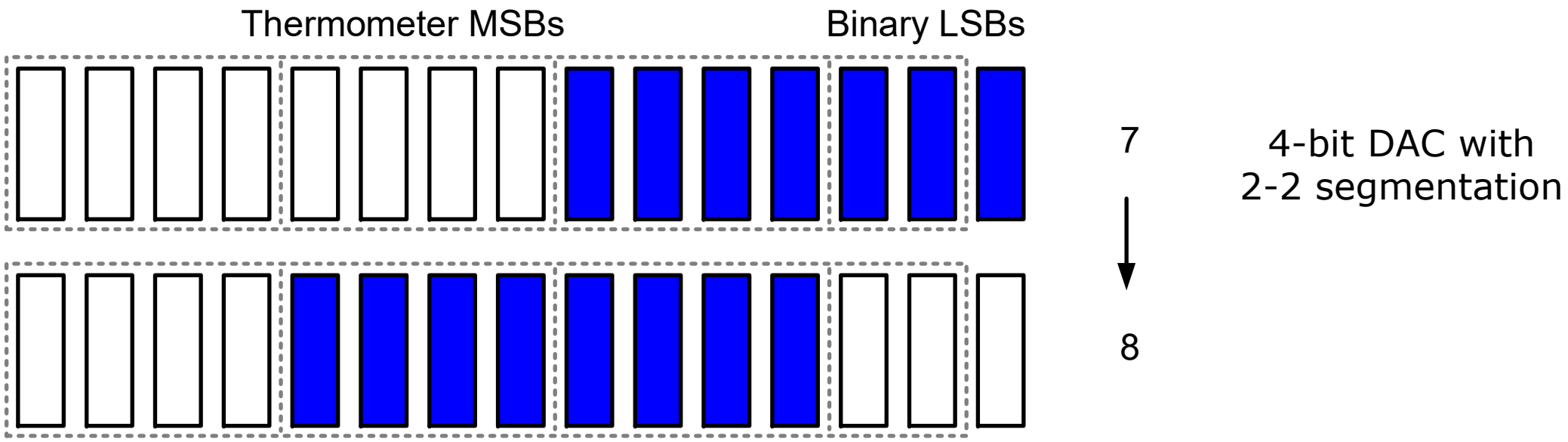
$$SFDR \geq \frac{3}{2}\frac{T_s}{\Delta t}$$

Update Rate (f_s)	SFDR Target	Tolerable skew (Δt)
1 GS/s	60 dB	1.5 ps
10 GS/s	60 dB	150 fs
64 GS/s	40 dB	230 fs

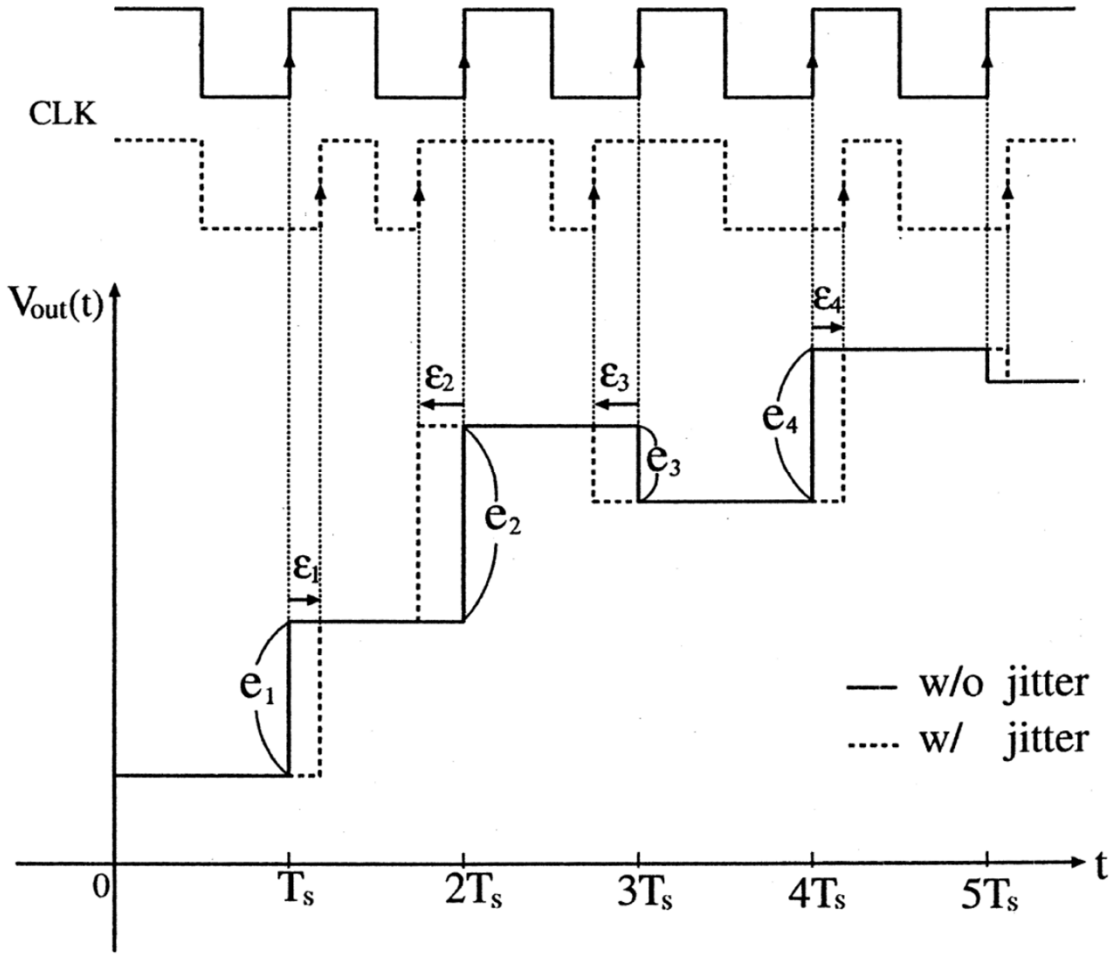
- Skew requirements not manageable in practice
- Hence, most high-speed DACs use other grouping strategies

Alternative Grouping Strategies

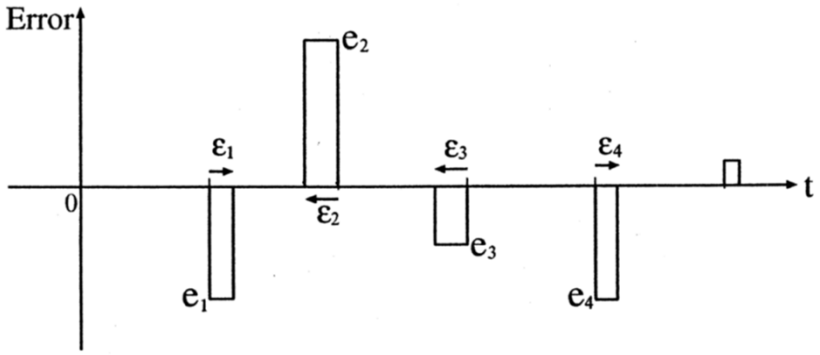
- No grouping ("thermometer DAC") is typically impractical
  - Large decoder, too many wires
- Typically look for golden middle: LSBs binary, MSBs thermometer encoded
  - More in Gabriele Manganaro's presentation



Global Clock Jitter (NRZ DAC)

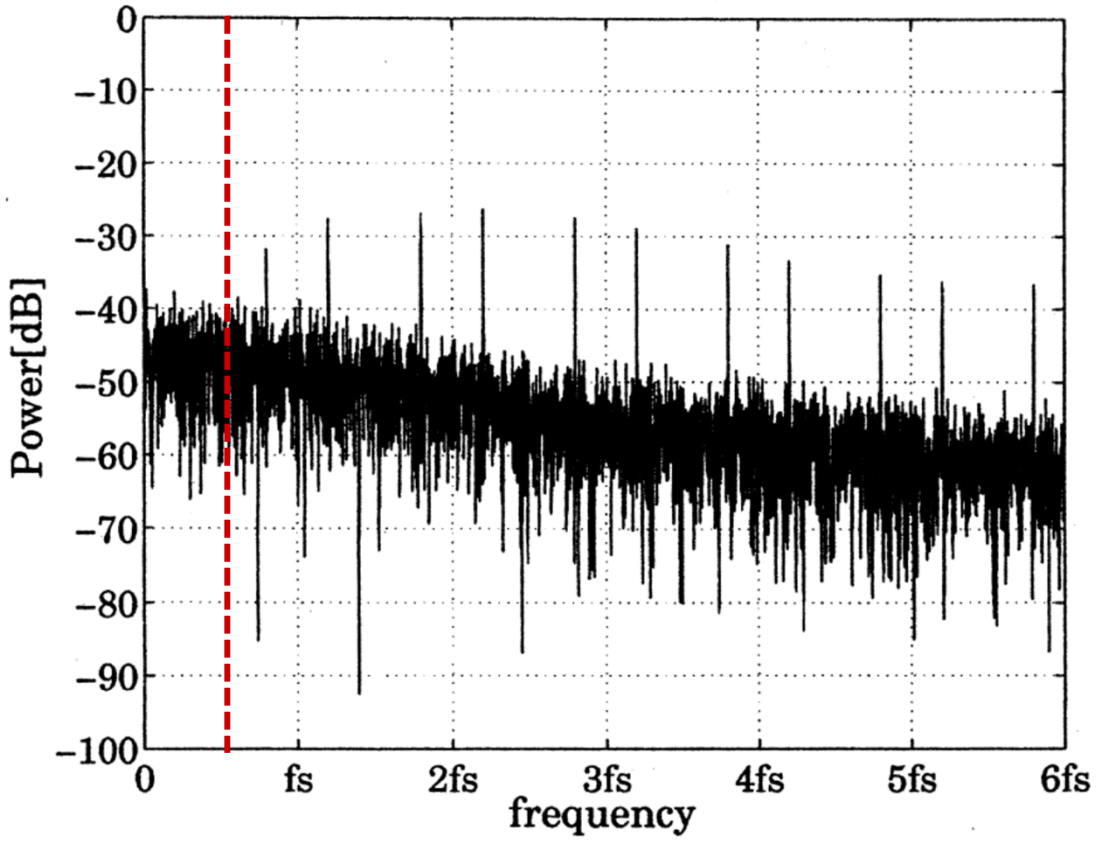


Error pulses with random width



[Kurosawa, 2002], [Kim 2018]

Error Spectrum



[Kurosawa, 2002]

- Spurious components lie outside first Nyquist zone
- In-band SNR (between 0…$f_s/2$) follows from same equation as ADC sampling jitter

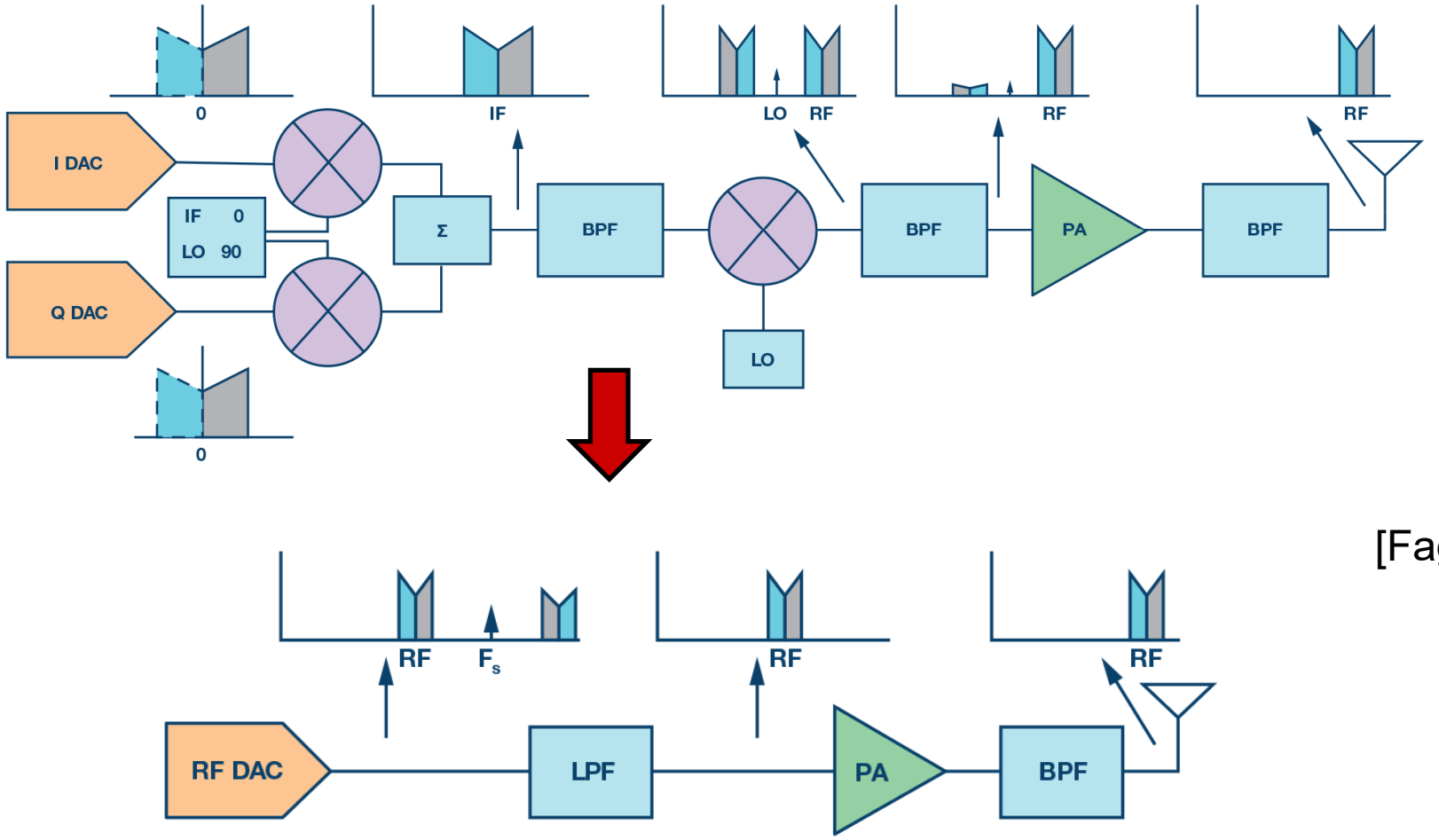
$$SNR_{jitter} \approx \frac{1}{\omega_{sig}^2 \sigma_t^2}$$

- Example
  - f_{sig} = 5 GHz, σ_t = 100 fs
  - SNR_{jitter} = 50 dB

Application Classes and Specs

- Traditional precision and baseband applications
  - Static errors like offset, DNL, INL
  - THD, SFDR
- RF DACs
  - Noise spectral density (NSD)
  - Intermodulation distortion (IM3, also called IMD or IMD3)
    - SFDR impairments are out of band (reduced by equipment & DAC's finite BW)
- DAC-based wireline transmitters
  - Eye diagram quality metrics (random jitter, etc.)
  - In-band SNDR

Heterodyning versus Direct RF Synthesis



[Fague, 2016], [Engel 2012]

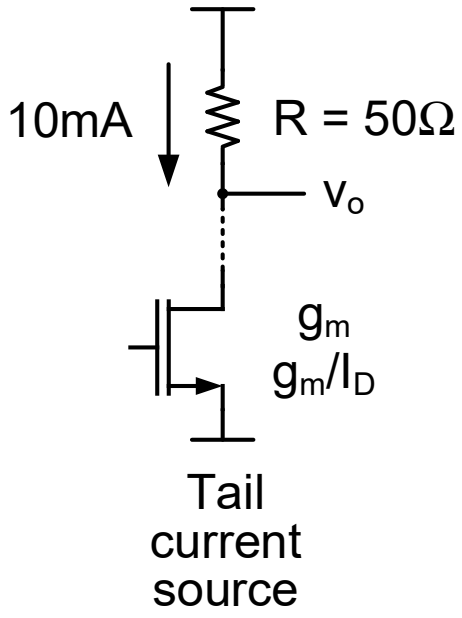
State-of-the-Art RF DAC

Process node	nm	16
Resolution	b	16
Sampling Rate	GS/s	6
Supply	V	1.0/3.0
Full Scale	mA	40
Area	mm^2	0.52
Power	mW	350
IMD@1.9GHz	dBc	-91
IMD@3.9GHz	dBc	-80
SFDR@0.4GHz	GHz	88
SFDR@2GHz	dBc	74
NSD@250MHz FS=3.5dBm	dBm/Hz	-165 (DEM=0) -162 (DEM=1)
NSD@2.6GHz FS= -3.7dBm	dBm/Hz	-162 (DEM=0) -159 (DEM=1)

[Lin, ISSCC 2018]

- IMD set by
  - Unit element matching
  - Segmentation scheme
  - Calibration and dynamic element matching (DEM) schemes
- NSD set by
  - Thermal noise
  - Jitter
  - Quantization noise (small for 16b)
  - DNL noise, DEM noise

Thermal NSD



$$\frac{\overline{v_o^2}}{df} = 4kTR(1 + g_m R) = 4kTR\left(1 + \frac{g_m}{I_D} I_D R\right)$$

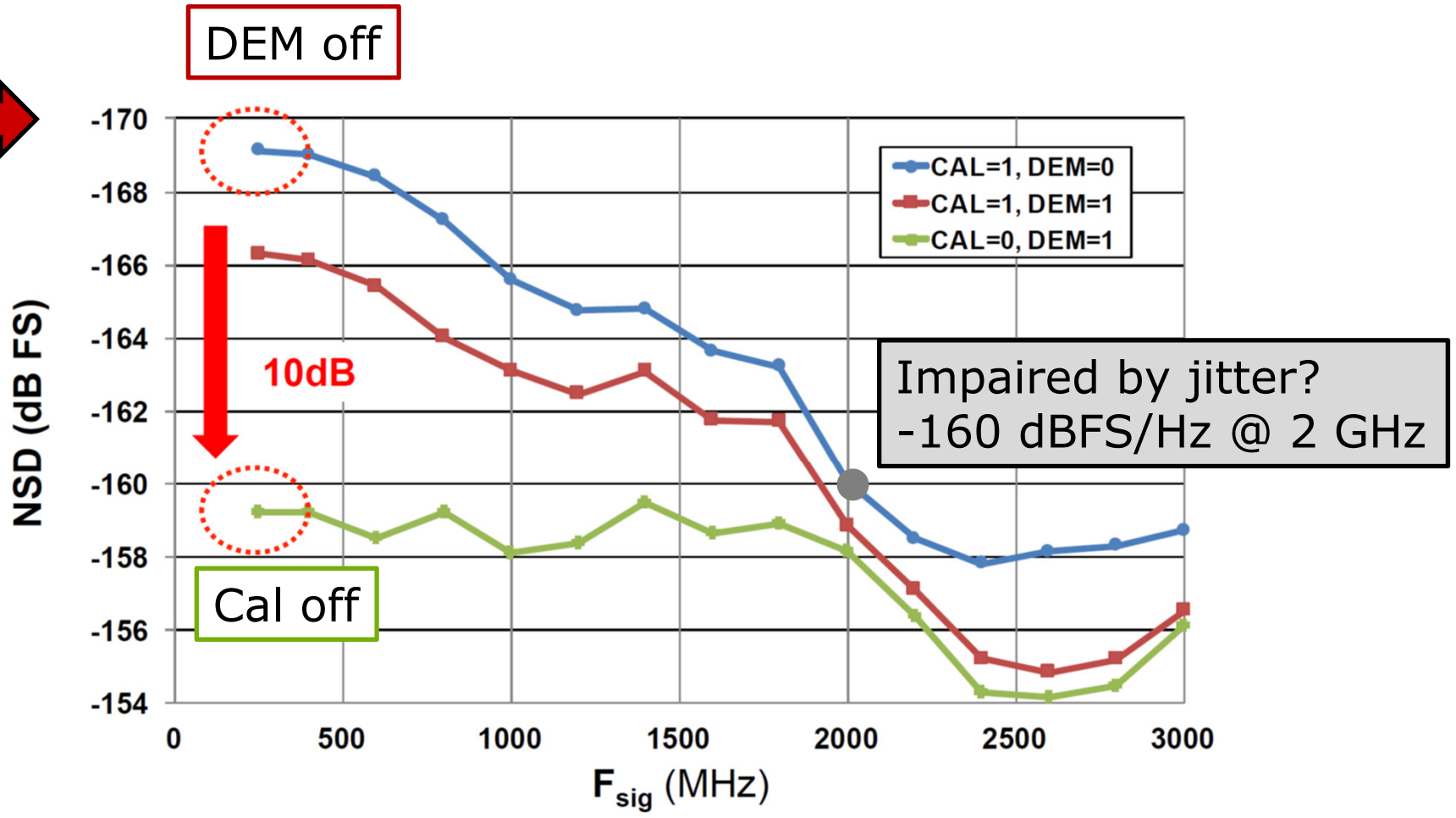
$$NSD_{th} = -174\frac{dBm}{Hz} + 10\log\left(\frac{g_m}{I_D} I_D R\right)$$

Example: $\frac{g_m}{I_D} I_D R = 10\frac{S}{A} \times 10mA \times 50\Omega = 5$

$$\Rightarrow NSD_{th} = -167\frac{dBm}{Hz} = -170.5\frac{dBFS}{Hz}$$ @FS=3.5 dBm

Measured NSD

Thermal limit



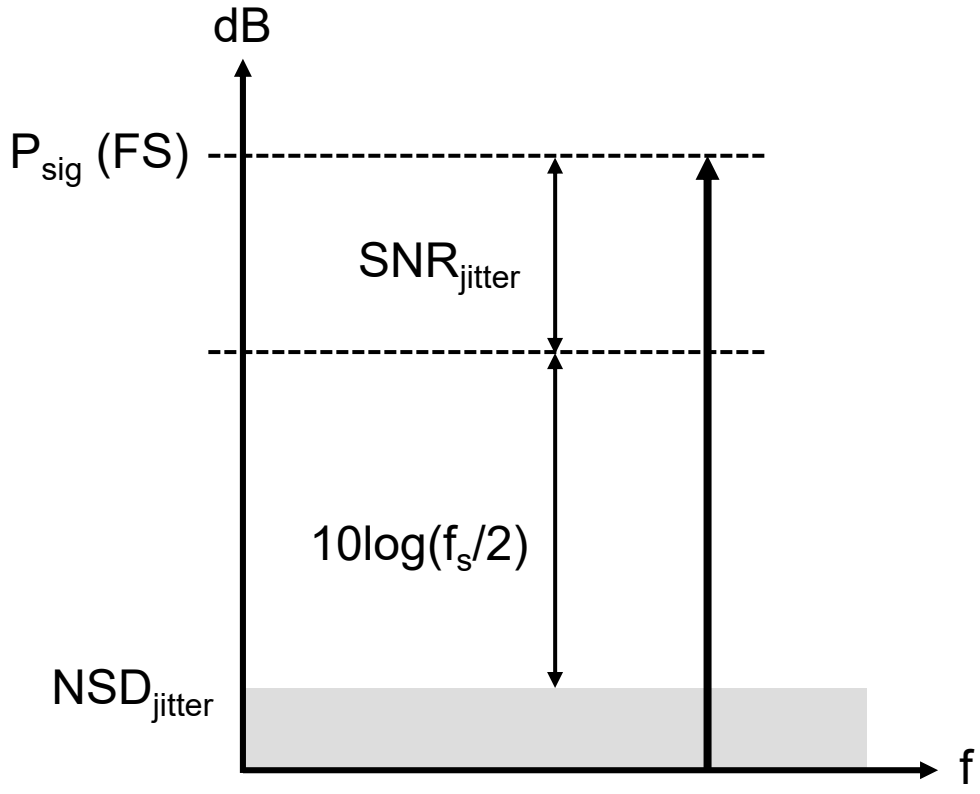
Jitter NSD

$$SNR_{jitter} \approx \frac{1}{\omega_{sig}^2 \sigma_t^2} = \frac{1}{(2\pi \times 2GHz \times 50fs)^2} = 64dB$$

$$NSD_{jitter} \approx P_{sig} - SNR_{jitter} - 10\log\left(\frac{f_s}{2}\right)$$

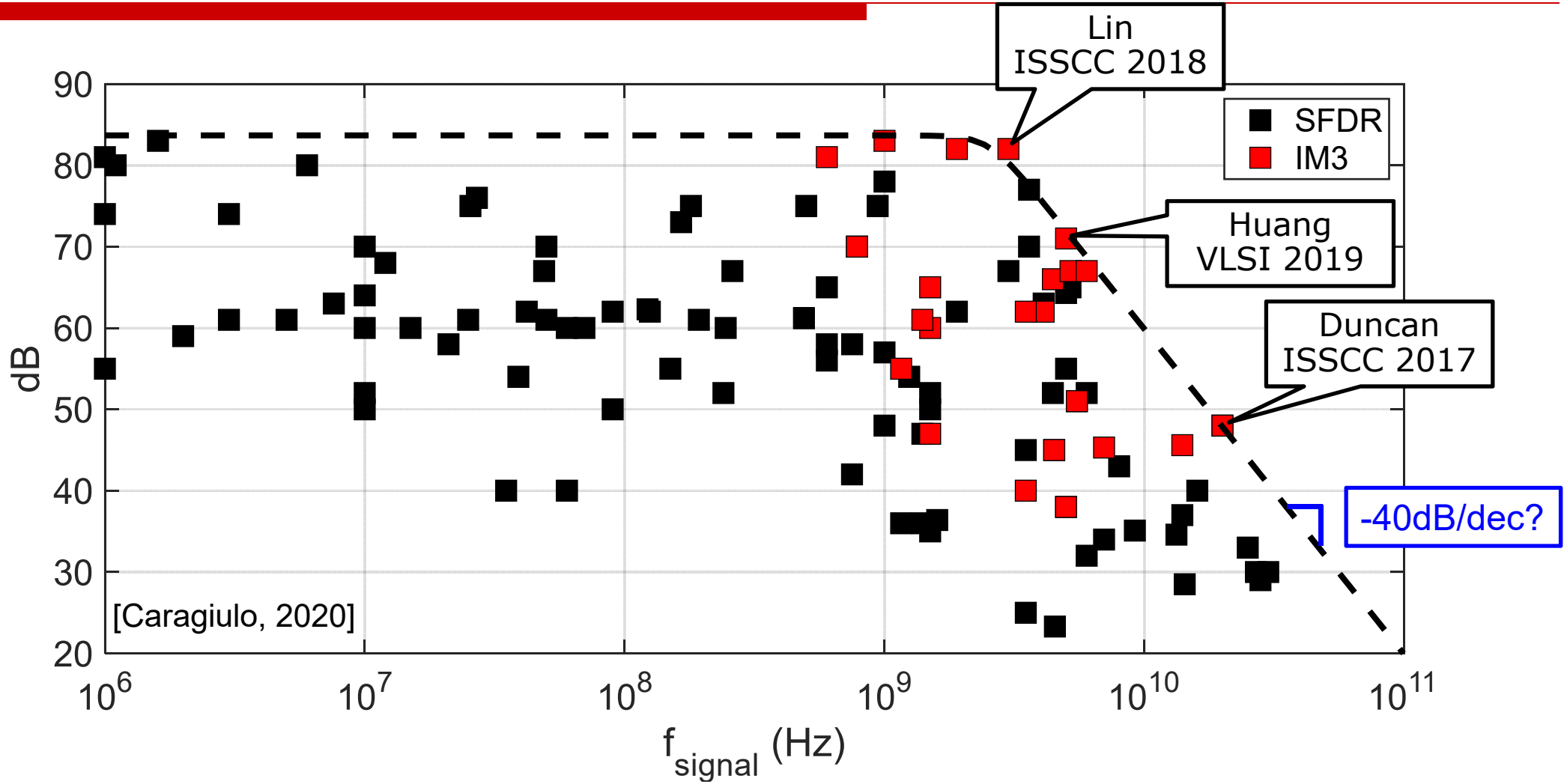
$$NSD_{jitter} \approx P_{sig} - 64dB - 10\log\left(\frac{6GHz}{2}\right)$$

$$NSD_{jitter} \approx -159\ dBFS/Hz$$



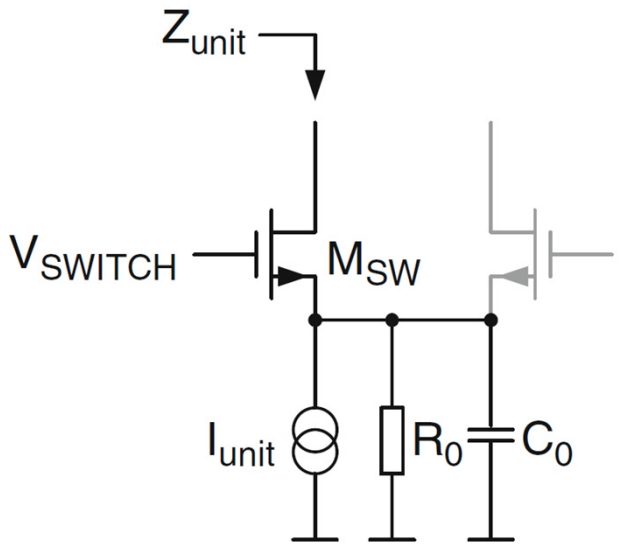
- Very difficult to improve this DAC further!

DAC Performance Survey

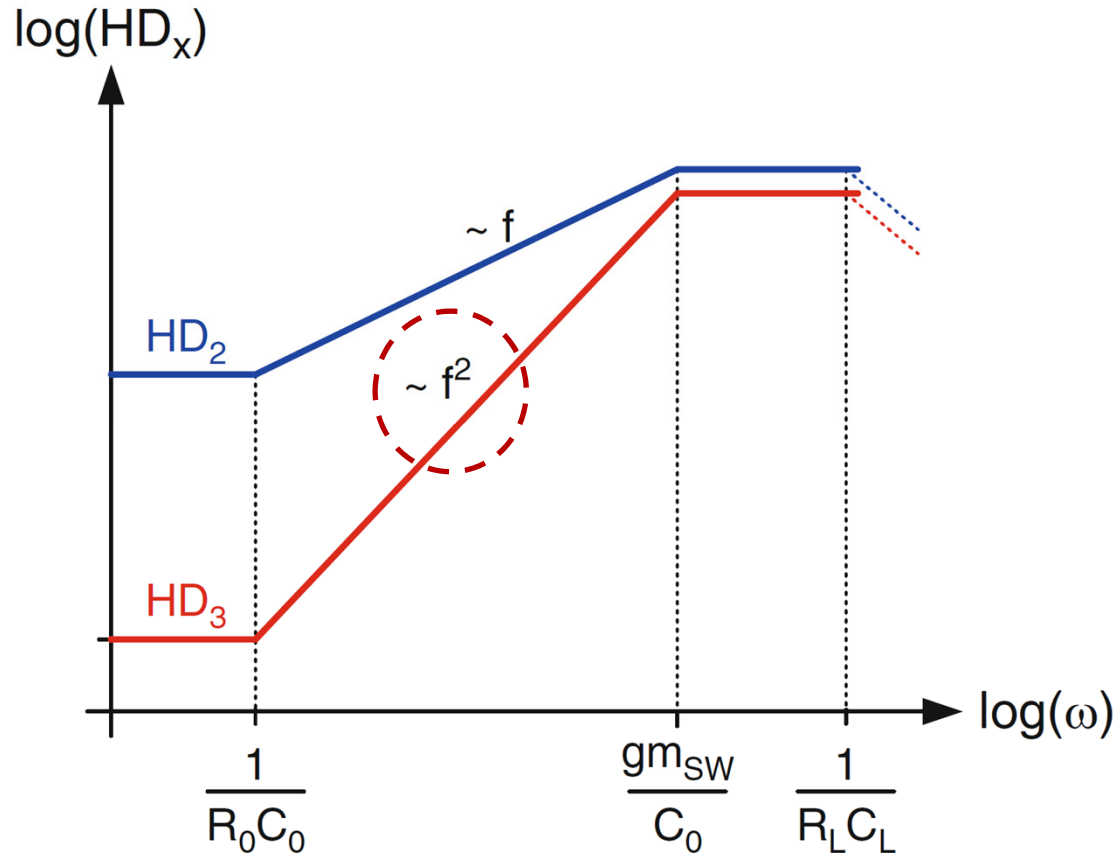


Possible Explanation for 40dB/dec Roll-Off?

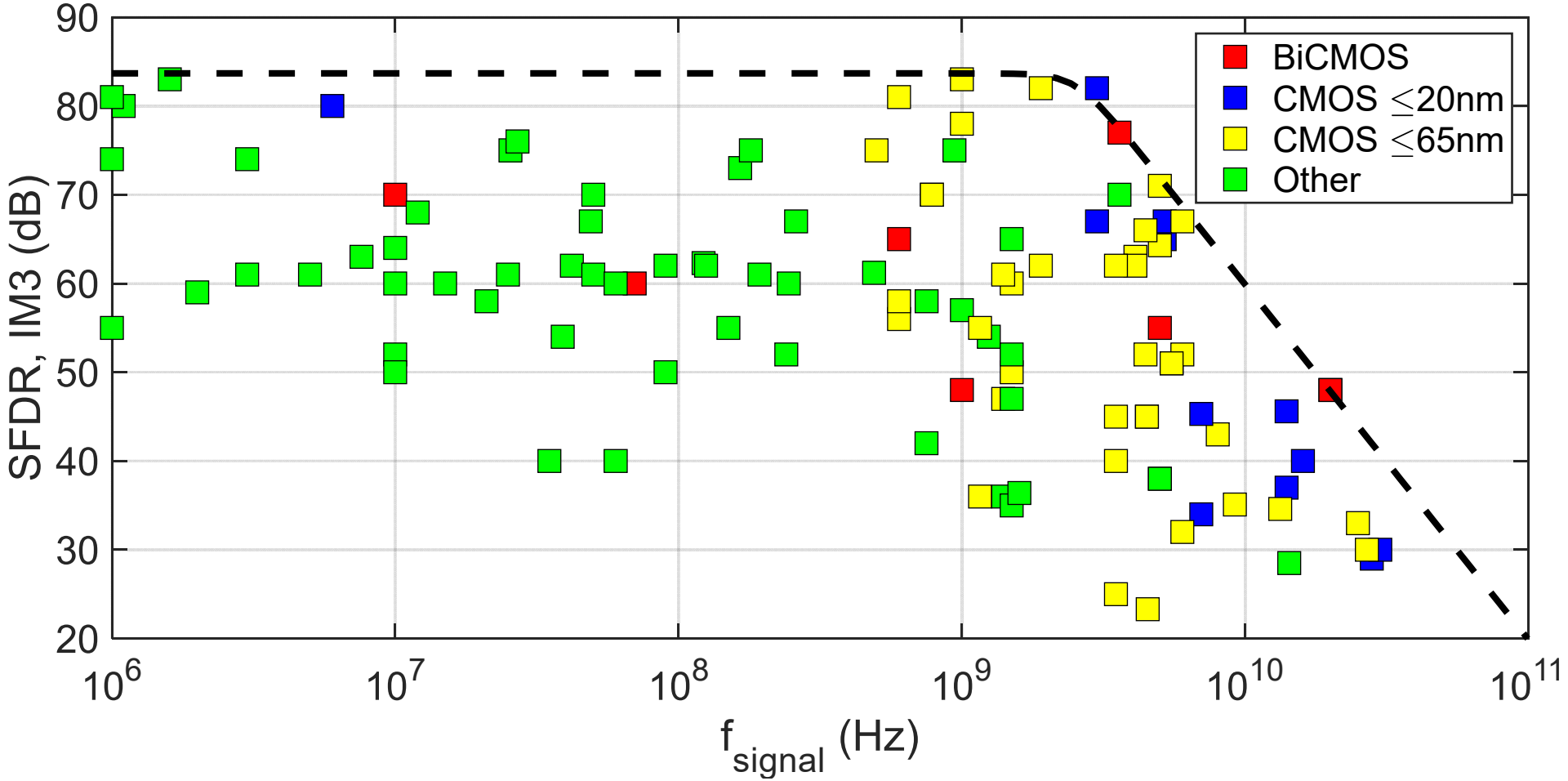
Time varying impedance



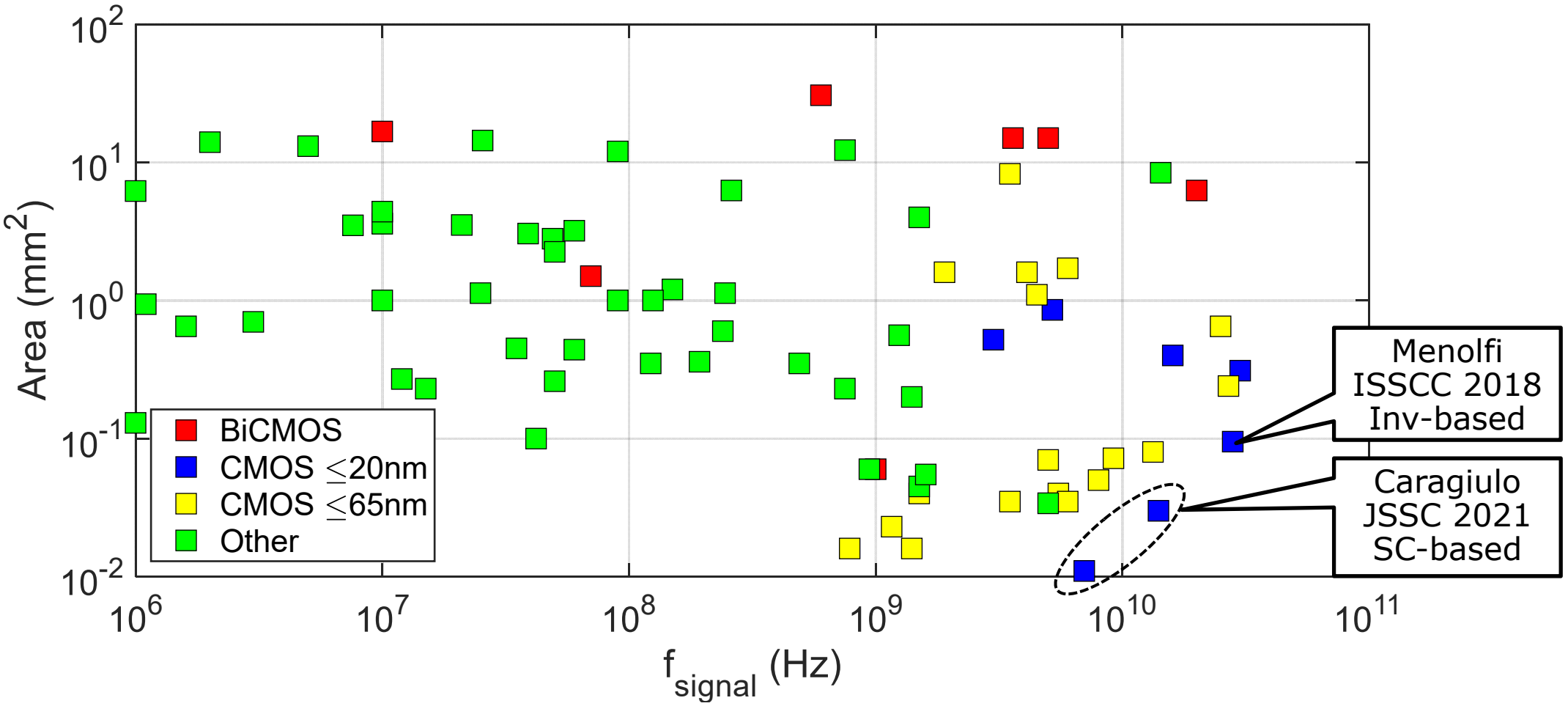
[Clara, 2013], [van den Bosch, 1999]



DAC Technology Landscape



DAC Area

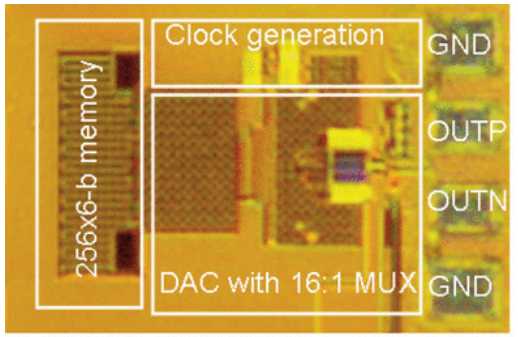


CS DAC Area Scaling?

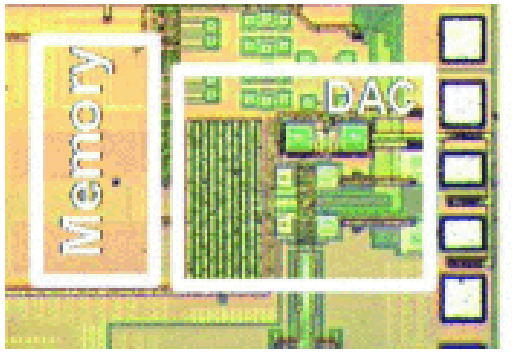
Greshishchev
BCICTS 2019

Greshishchev
ISSCC 2011

	This Work	[5]	[6]	[4]
Technology	7nm	14nm	20nm	65nm
Sampling Rate (GS/s)	60	56	64	56
Resolution	8b	8b	8b	6b
SINAD (dB)	29.5	n/a	n/a	27.7
Full Scale Output	800 mVppd	920 mVppd	700 mVppd	600mVppd
Switch	CML	SST	CML	CML
Supply Voltage (V)	0.9 + 1.9	0.95	1 + 1.8	1.1 + 2.5
Power Consumption	560 mW (Memory included)	286 mW	620 mW	750 mW



65nm → 0.24 mm^2



7nm → 0.31 mm^2

Some Take-Aways

- Symbiotic interplay between technology push and application pull has led to remarkable performance gains in data converters
- Today's data converters operate close to practical limits
  - Low-speed ADCs: 8kT×SNR energy limit
  - High-speed ADCs and DACs: Tens of femtoseconds timing jitter
- Architecture trends
  - ADCs: Going hybrid & dominance of SAR-based architectures
  - DACs: Current steering dominates, but some alternatives emerging
- Application trends
  - RF ADCs and DACs
  - Ultra-high-speed wireline ADCs and DACs

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